ATTACHMENT B

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UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF CALIFORNIA

VIASAT, INC. a Delaware corporation, Plaintiff and Counter-Defendant, v. ACACIA COMMUNICATIONS, INC. a Delaware corporation, Defendant and Counter-Claimant.	Case No. 3:16-463-BEN-JMA **Declaration of Erika H. Warren in Support of ViaSat's Motion for Summary Judgment for Patent Misappropriation** Date: March 5, 2018 Time: 10:30 a.m. PST Place: Courtroom 5A Hon. Dist. Judge Roger T. Benitez Hon. Magistrate Judge Jan M. Adler Case Initiated: January 21, 2016

I, Erika H. Warren, declare as follows:

1. I am an attorney licensed to practice in the State of California, and an attorney at the law firm of Warren Lex LLP, counsel for ViaSat, Inc. ("ViaSat") in this action. I have personal knowledge of the matters set forth herein and, if called as a witness, could and would testify competently thereto.

2. Attached as Exhibit 1 is a true and correct copy of provisional U.S. patent application no. 61/435,278, filed on January 22, 2011.

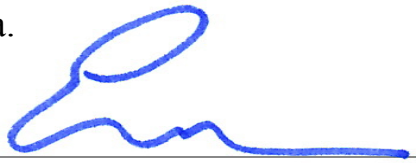
3. Attached as Exhibit 2 is a true and correct copy of provisional U.S. patent application no. 61/521,263, filed on August 8, 2011.

4. Attached as Exhibit 3 is a true and correct copy of the IP Core Development and License Agreement between ViaSat and Acacia, dated November 20, 2009, which is Exhibit A to ViaSat's Complaint in this action.

5. Attached as Exhibit 4 is a true and correct copy of the October 27, 2017 Expert Report of Dr. Paul Prucnal, served by Acacia in this action. This exhibit is filed under seal based on ViaSat's concurrently filed Motion to File Under Seal Documents in Support of Motion for Summary Judgment on Acacia's Counterclaim for Patent Misappropriation.

6. Attached as Exhibit 5 is a true and correct copy of excerpts from the deposition transcript of Dr. Paul Prucnal, dated December 4, 2017. This exhibit is filed under seal based on ViaSat's concurrently filed Motion to File Under Seal Documents in Support of Motion for Summary Judgment on Acacia's Counterclaim for Patent Misappropriation.

I declare under penalty of perjury that the foregoing is true and correct. Executed on February 2, 2018, in San Francisco, California.



Erika H. Warren

CERTIFICATE OF SERVICE

I certify that today I am causing to be served the foregoing document by CM/ECF notice of electronic filing upon the parties and counsel registered as CM/ECF Users. I further certify that am causing the foregoing document to be served by electronic means via email upon counsel for Acacia Communications, Inc., per the agreement of counsel.

Dated: February 2, 2018

s/ *Kenneth M. Fitzgerald*
Kenneth M. Fitzgerald, Esq.

Exhibit 1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/435,278	01/22/2011		220	ECC-0452-US		

CONFIRMATION NO. 5581

FILING RECEIPT

31864
VIASAT, INC.
C/O Stacy Nguyen
PATENT DEPARTMENT
6155 EL CAMINO REAL
CARLSBAD, CA 92009

OC000000046523312

Date Mailed: 03/15/2011

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Sameep Dave, Cleveland, OH;
Fan Mo, Cleveland, OH;
William Thesling, Cleveland, OH;
Matthew Nimon, Cleveland, OH;
Lawrence Esker, Cleveland, OH;
Yuri Zelensky, Cleveland, OH;

Power of Attorney:
Charles Pateros--50677

If Required, Foreign Filing License Granted: 03/11/2011
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/435,278**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
Title

High Rate Optical Communication

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international

application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Doc Code: TR.PROV
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

Inventor 1 — Remove

Given Name	Middle Name	Family Name	City	State	Country
Sameep		Dave	Cleveland	OH	US

Inventor 2 — Remove

Given Name	Middle Name	Family Name	City	State	Country
Fan		Mo	Cleveland	OH	US

Inventor 3 — Remove

Given Name	Middle Name	Family Name	City	State	Country
William		Thesling	Cleveland	OH	US

Inventor 4 — Remove

Given Name	Middle Name	Family Name	City	State	Country
Matthew		Nimon	Cleveland	OH	US

Inventor 5 — Remove

Given Name	Middle Name	Family Name	City	State	Country
Lawrence		Esker	Cleveland	OH	US

Inventor 6 — Remove

Given Name	Middle Name	Family Name	City	State	Country
Yuri		Zelensky	Cleveland	OH	US

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Title of Invention	High Rate Optical Communication
Attorney Docket Number (if applicable)	ECC-0452-US

Correspondence Address

Direct all correspondence to (select one):

◉ The address corresponding to Customer Number	○ Firm or Individual Name

Doc Code: TR.PROV
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Customer Number	31864

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.
◉ No.
○ Yes, the name of the U.S. Government agency and the Government contract number are:

Doc Code: TR.PROV
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Entity Status

Applicant claims small entity status under 37 CFR 1.27

○ Yes, applicant qualifies for small entity status under 37 CFR 1.27

◉ No

Warning

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Dr. Charles Nicholas Pateros #50,677/			Date (YYYY-MM-DD)	2011-01-22
First Name	Charles	Last Name	Pateros	Registration Number (If appropriate)	50677

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **This form can only be used when in conjunction with EFS-Web. If this form is mailed to the USPTO, it may cause delays in handling the provisional application.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, t o a n other federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PROVISIONAL APPLICATION FOR PATENT

TITLE: High Rate Optical Communication
INVENTORS: Sameep Dave, Fan Mo, Bill Thesling, Matt Nimon, Lawrence Esker, Yuri Zelensky
DOCKET: ECC-0452-US
DATE: January 22, 2011

Cross Reference to Related Applications

NOT APPLICABLE

Federal Research Statement

NOT APPLICABLE

Background of Invention

While fiber optic channels are considered very good for data transmission, this assumption breaks down at high rates such as 40-100 Gbps and beyond. At these rates, new modulation, demodulation and error correction techniques are required.

Summary of Invention

Enabling technologies for the successful transmission and reception of high rate digital signals over optical channels are presented. Implementation strategies for low-complexity, easily realizable systems are also disclosed. Although the solutions are presented in the context of an optical transport environment, the techniques and embodiments have applicability across a wide spectrum of applications.

Detailed Description

A typical optical data transport system will comprise a data source, a data transport layer (framer), a FEC coder, a modulator, a transmitter fiber interface, a fiber connection, a receiver fiber interface, a demodulator, a FEC decoder, a data transport layer de-framer, and a data sink (user). This document will focus primarily on the demodulator and FEC decoder, but solutions presented will impact the design and implementation of other system components.

Digital Demodulator architecture for 40 / 100 Gbps OTN and beyond

Problem 40 / 100 Gbps OTN systems require a digital demodulator to reliably receive the signals at the receiver

The high data rates make the receiver design very complex as very high degree of parallelism is required

Optical channel presents a variety of unique impairments like CD, PMD, PDL and other types of distortions that need to be tracked / corrected digitally

Solution An architecture for a digital receiver that can demodulate the signal in presence of the various optical impairments with very low implementation loss and reasonable implementation complexity that allows for implementation in latest technology ASICs

Technical Keywords OTN, 40 / 100 / 400 / 1000 Gbps, Demodulator, Equalizer, DSP

Novel This is a new demodulator design that can process the signal with all the optical impairments in a highly parallel fashion while keeping reasonable implementation complexity.

Inventors Fan Mo, Bill Thesling, Matt Nimon and Sameep Dave

Digital Demodulator architecture for 40 / 100 Gbps

The Digital Demodulator processes the samples of the analog I and Q components of the two polarization components to recover the transmitted data. At the input side the Demodulator accepts four parallel streams carrying HI (Horizontal I), HQ (Horizontal Q), VI (Vertical I) and VQ (Vertical Q) samples. Each stream will contain multiple samples per clock.

At its output the Demodulator provides demodulated hard-decision data to the HDFEC decoder. The Demodulator may or may not identify the beginning of a FEC frame depending upon the mode of operation. Additionally the Demodulator may receive feedback signals from an internal or external (to the ASIC) HDFEC Decoder regarding the convergence status.

The top level demodulator design is show in Figure 1.

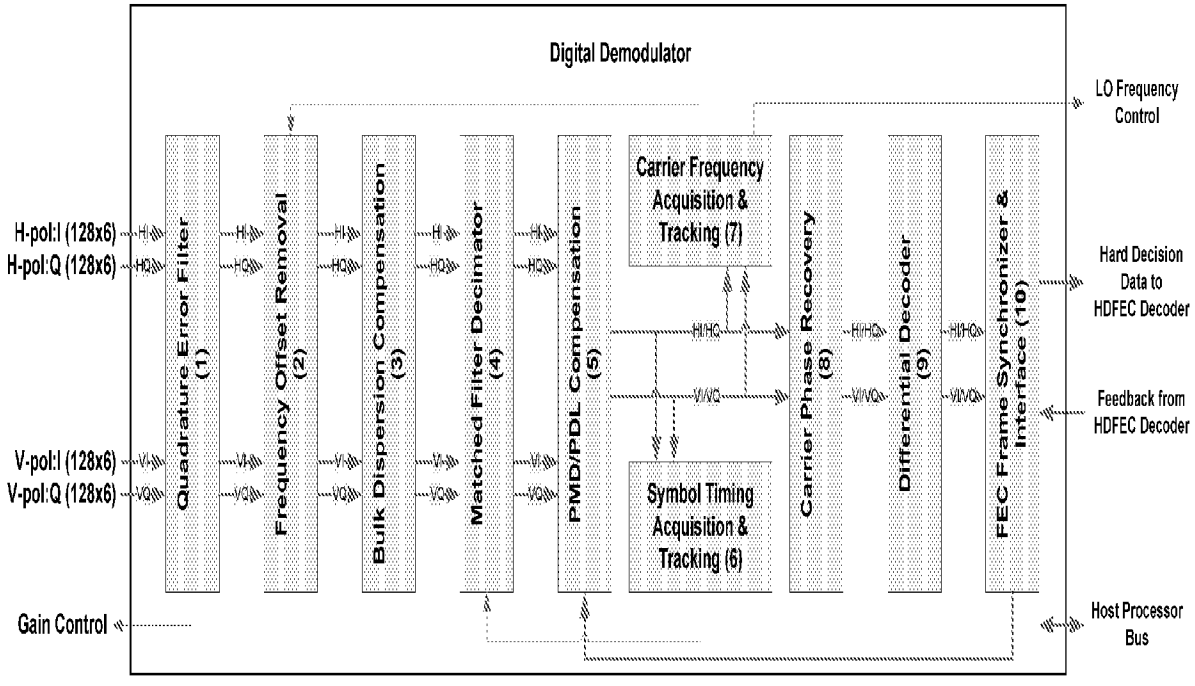


Figure 1: Demodulator Top Level Block Diagram

The Demodulator may have a control and monitor interface bus connected to a host processor allowing for configuration of demodulator parameters (filter coefficients, loop gains, etc.) and extraction of demodulator status.

The following sections detail the functional specification for the major sub-modules within the demodulator design.

Quadrature Error Filters

The Quadrature Error Filter (QEF) module provides a collection of miscellaneous data formatting, error detection and correction functions. Figure 2 shows the top level functional block diagram for the QEF module.

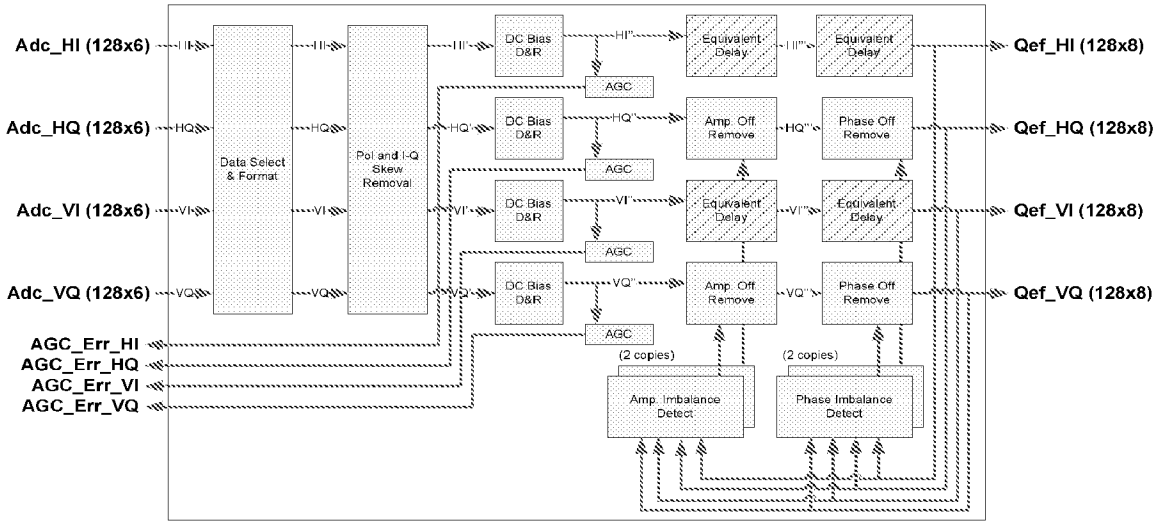


Figure 2: Quadrature Error Filters Top Level

Input data samples are expected to be in binary-offset / offset-binary format coming in from the ADC and it will be converted to the required 2's complement (2C) format for the processing inside the DSP.

The incoming HI, HQ, VI and VQ streams also can be independently swapped and inverted if needed. This allows compensating for any design issues that might translate into an accidental inversion or IQ swap.

Each data stream is processed through a skew correction block to remove polarization skew (between H and V poles) as well as I-Q skew within a pole.

For polarization skew removal a delay element will be used that can delay the poles with respect to each other by a programmable number of integer sample durations. Shift values up to +/- 4 samples will be supported on each pole for a maximum relative offset of +/- 8 samples. This will allow coarse polarization skew removal at calibration time. Any residual sub-sample duration polarization skew at calibration time or any slow time variation in the polarization skew will be tracked out by the PMD equalizer. Please note that this control will be available independently on the I and Q streams within a polarization to help coarse I/Q skew removal.

The QEF module provides for detection and removal of four types of quadrature signal errors: I/Q Skew, DC bias, I/Q amplitude imbalance, and I/Q phase imbalance. All four error detectors can be independently enabled or disabled via the APB processor interface, and the detected error values are output as status values via this same interface.

Frequency Offset Removal

The Frequency Offset Removal (FOR) module will perform a frequency rotation on the data samples coming out of the QEF module. The amount of frequency rotation is controlled by the frequency error input that is sourced by the Carrier Frequency Acquisition and Tracking (CFAT) module. This frequency offset removal function is only intended to remove residual frequency left from the LO laser tuning in the optical domain.

Figure 3 shows the top level block diagram for the frequency offset removal.

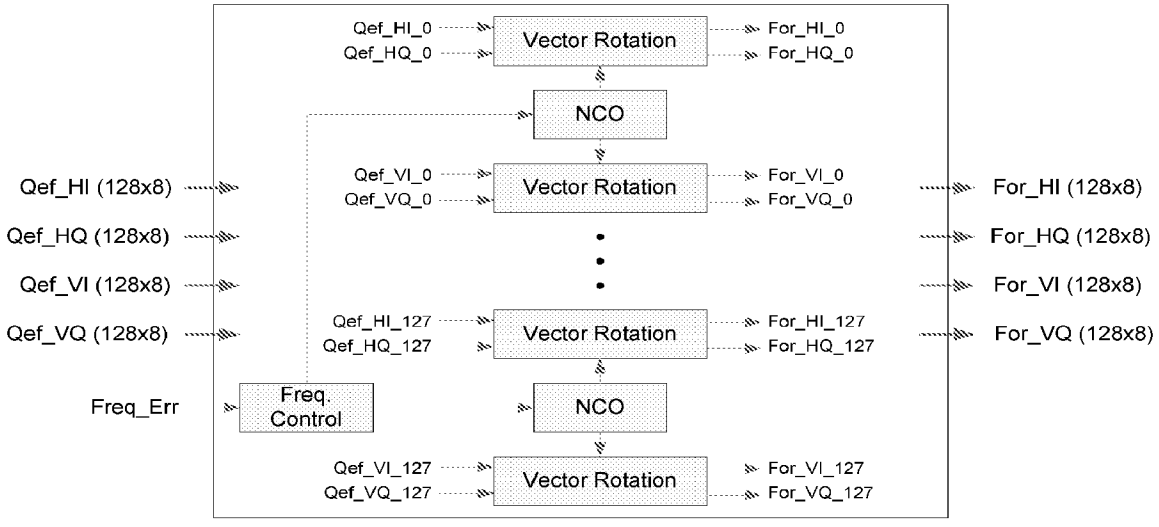


Figure 3: Frequency Offset Removal Top Level

Bulk Dispersion Compensation

The Bulk Dispersion Compensation module removes the bulk Chromatic Dispersion (CD) from the horizontal and vertical polarization channels. The compensation is applied via a filter in the frequency domain. The amount of CD correction is controlled by the CD filter inputs that are derived outside of the demodulator and provided via the host processor control and monitor interface. Figure 4 shows an example top level block diagram for the module.

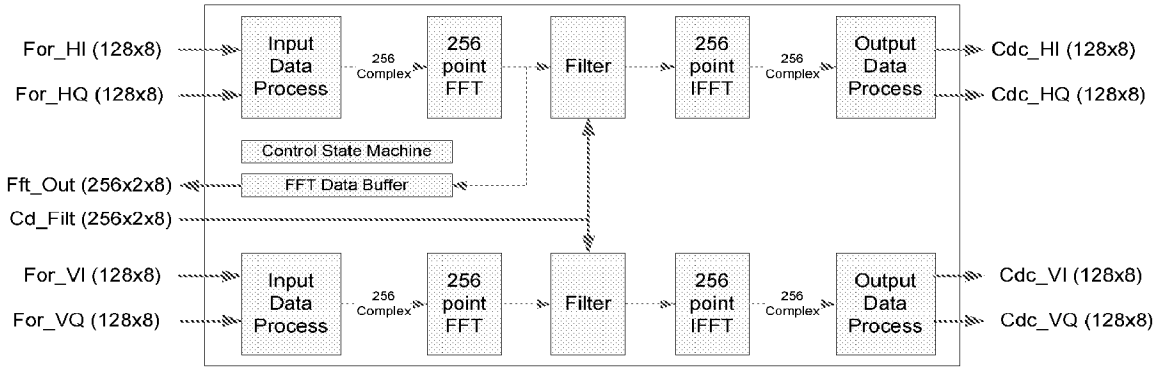


Figure 4: Bulk Dispersion Compensation Top Level

The CD compensation (CDC) for any given sample requires 'input' from a range of data samples before and after the sample.

The Horizontal and Vertical I/Q data pairs are processed through two independent, equivalent processing paths. A single control state machine provides the proper enable and block alignment logic to all other blocks in the module.

The output of the FFT is complex frequency domain data. This data is input to the filter block where a frequency domain filtering operation is performed. The complex FFT outputs are also sent to a data buffer to be read out via the control and monitor block. Note that this is just a snapshot buffer, only a single FFT result is required to be stored at any given time.

The output of the filter block is again complex pairs of CD corrected frequency domain data per clock. The data is input to the 256-point IFFT for conversion back to the time domain. The state machine controls the flow of data through the IFFT.

Matched Filter Decimator

The Matched Filter Decimator (MFD) module implements an interpolation function that provides decimation from the ADC sample rate to 2x the symbol rate. Each of the four

data streams has an independent bank of FIR filters with fixed coefficients. The filter coefficients implement a Raised Cosine (RC) low-pass filter with roll-off of 0.4. The symbol timing error input value fine tunes the decimation rate such that one of the two samples per symbol output is an on-time sample. The sample block assembler takes in the data samples from the filter bank and groups the samples such that valid data output from the MFD block always contains 0 or 128 data samples per clock per stream. Note that valid output data is not available on each clock and the data valid output indicates when valid output data is available. The top level MFD design is shown in Figure 5.

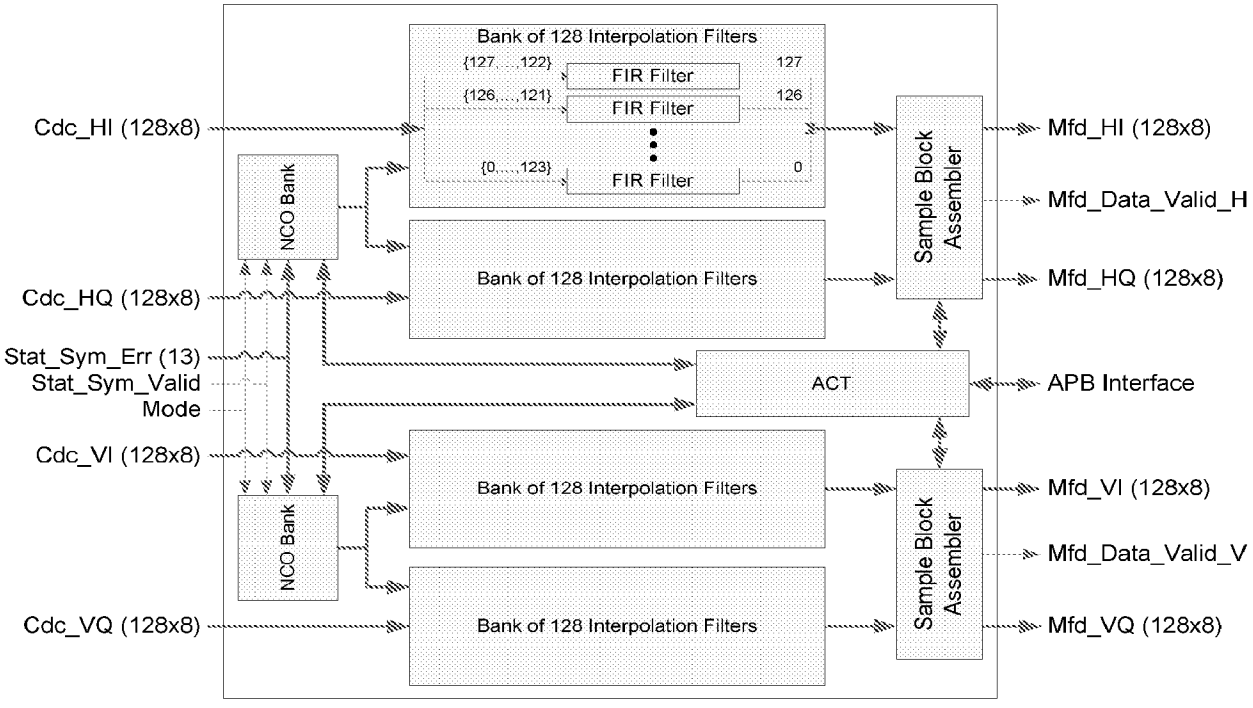


Figure 5: Matched Filter Decimator Top Level

The symbol error is a signed value providing for a maximum symbol timing correction capability of certain % of the baud rate. The symbol timing error is input to the NCO bank where it is added to a nominal NCO step value to produce a corrected NCO step. The nominal NCO step values are pre-computed and fixed for the nominal symbol rates and selected via a configuration register in the ACT block. The corrected NCO step value is also reported as status.

There are four banks of interpolation filters in the module with each banks processing one of the data streams. Each filter bank takes in one data word of sample data and an array of interpolation phases per clock. The filter blocks filter the incoming data through the filter banks with the interpolation phase for each filter driven by the corresponding

interpolation phase value. The filter bank produces 2 samples per symbol out for each data stream.

The decimation rate is controlled by a NCO so the number of output samples produced per clock is not a constant. In order to simplify data processing through the remainder of the Demodulator, data samples are gathered and assembled into blocks of fixed number of samples per stream per clock by the sample block assembler. The assembly function is identical for the I and Q streams in each polarization so one assembly block services two streams.

As the ratio of the output/input samples per clock is not exact, there will be clock cycles where the MFD does not output any data. The Mfd_Data_Valid_x output is asserted only on clocks with valid output data.

The MFD design is optimized for a particular decimation factor. So the ADC sample rate has to be close to $2 + \varepsilon$ times the symbol rate. The ε will be 0.009 for the Polo design.

PMD/PDL Compensation

The PMD/PDL compensation module utilizes adaptive equalization to compensate for the cross polarization interference, IQ channel interference, adjacent symbol interference introduced by PMD and PDL in optical channel and other residual impairments (like residual CD). The adaptive equalizer (EQ) takes in data at 1 or 2 samples/symbol from the MFD and processes the data through a bank of FIR filters with adaptive filter tap coefficients. The top level block diagram for this module is shown in Figure 6.

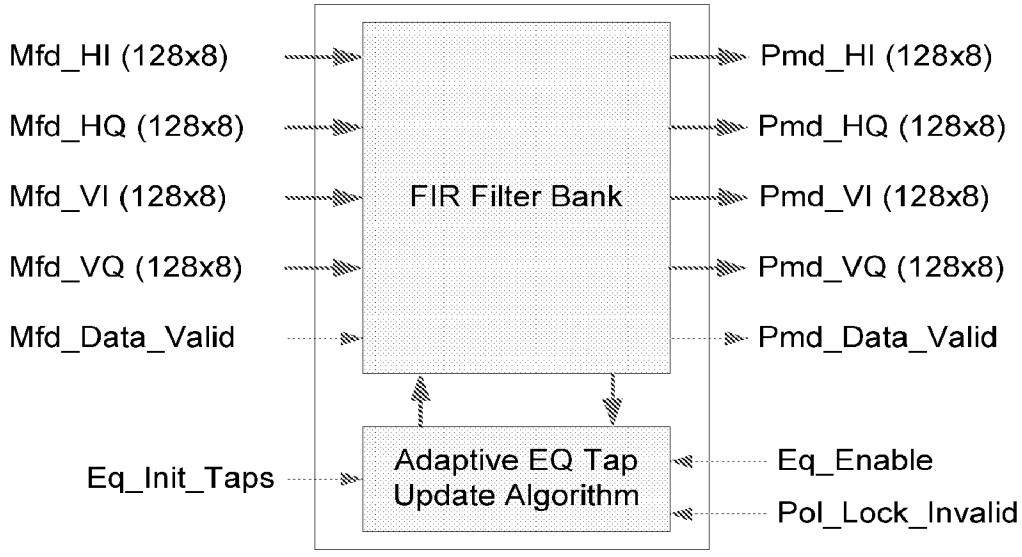


Figure 6: PMD/PDL Compensation Top Level

The FIR filter bank consists of four, 16-tap real or complex filters operating at 1 or 2 taps per symbol. A conceptual view of the filter bank is shown in Figure 7. Each quadrant in Figure 7 is a complex filter.

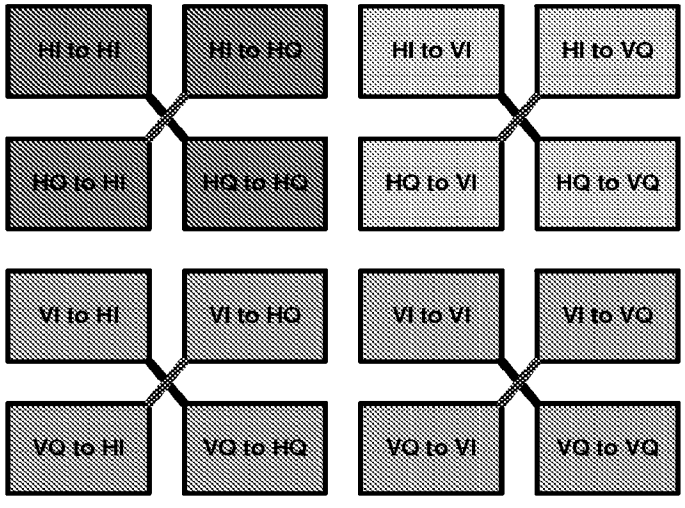


Figure 7: PMD Filter Bank

The filter taps can be initialized through the control and monitor interface. Generally the filters along the diagonal are initialized as all-pass filters with a center tap weight of 1.0

and all other taps set to 0.0. The rest of the filters are initialized with all zero tap weights. The taps are updated by the adaptive EQ tap update algorithm when enabled.

The adaptive EQ tap update algorithm may be a Constant Modulus Algorithm (CMA). This algorithm drives the constellation points on each polarization (at optimal symbol timing) to a circle with the desired radius with minimum radius variation.

The adaptive EQ will converge, with high probability, to a solution that properly decouples the two polarizations. There are however corner cases where the EQ will converge to output the same polarization on both polarization outputs. This error event is detected downstream by the FEC frame synchronizer. When the error is detected, the Pol_Lock_Invalid signal is asserted. The assertion causes the filter taps for the Vertical pole output to be reset.

The module generates all the on-time output samples but generates only half the off-time samples. This helps keep the design size smaller and is sufficient for the symbol timing tracking needs of the following modules.

Symbol Timing Acquisition and Tracking

Symbol Timing Acquisition and Tracking (STAT) may be achieved by means of an early/late symbol radius matching scheme and PI controller. This module also has a symbol timing lock detection mechanism that outputs a symbol lock indicator. There are two sets of gains for the PI controller (wide band for acquisition and narrow band for tracking). When not in timing lock, the wideband gains are used, otherwise, the narrowband gains are used. The top level design is shown in Figure 8.

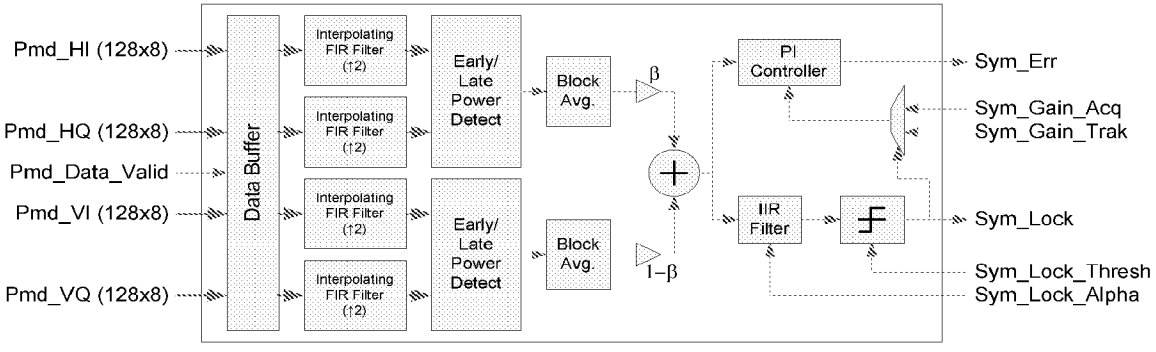


Figure 8: Symbol Timing Acquisition and Tracking Top Level

The incoming I and Q data at 2 samples/symbol represents data samples that are on-time and ½ of a symbol period off from on-time. Each of the incoming data sets (I and Q) is processed through two 12-tap interpolating FIR filters. The FIR filter coefficients are

fixed and have been designed such that one set of filters interpolates the data by ¼ of a symbol period early and the other set by ¼ of a symbol period late.

The early and late I/Q pairs from each polarization are input to a pair of early/late power detection modules. The symbol timing error in each polarization is calculated as the early radius value minus the late radius value. The raw error values are input to a pair of block averaging functions that average the errors.

The average error values from the two polarizations are multiplied by a weighting factor (β) and summed to produce an average symbol timing error for the combined dual-polarization signal. The nominal value for β is 0.50 but it can be programmed in the range {0.0, 1.0}.

The composite average error value is used to update a PI controller once per data block. The PI controller output is the symbol timing error that is fed back to the MFD to adjust the symbol timing. The PI controller gains are selected by the state of the Sym_Lock signal. When not in symbol lock, the wide band acquisition gains are used, otherwise, the narrow band tracking gains are used.

The composite average error value is also used to update an IIR filter. The output of the IIR filter is compared against a user configurable error threshold value. When the filter output drops below the threshold, symbol lock is declared.

Carrier Frequency Acquisition and Tracking

The Carrier Frequency Acquisition and Tracking (CFAT) module is responsible for acquiring as well as tracking carrier frequency. Carrier frequency acquisition is achieved by means of a FFT with appropriate averaging and peak frequency component detection. Carrier frequency tracking is achieved by means of a 2-point DFT with appropriate averaging and variable tracking bandwidth. The frequency error is processed through a PI controller to produce a filtered frequency error. CFAT module also has a carrier frequency lock detection mechanism that outputs a freq_lock indicator. When not in frequency lock, the wide DFT bandwidth is used, otherwise, the narrow DFT bandwidth is used. The freq_lock signal is also used to decide if the FEC frame synchronizer (FFS) module shall forward data to the decoder. The top level design is shown in Figure 9.

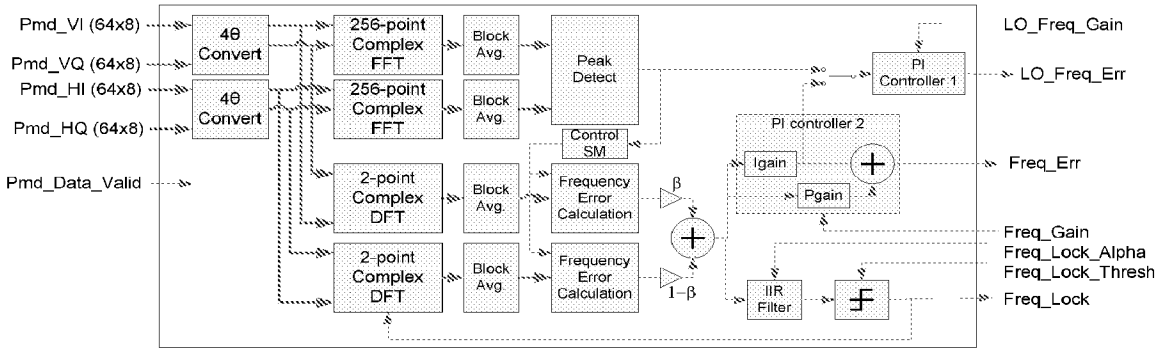


Figure 9: Carrier Frequency Acquisition and Tracking Top Level

The CFAT module operates on the on-time I/Q data samples from both polarizations.

To keep design complexity down, the module does not operate on all data samples, rather on blocks of contiguous symbols once every few clocks to allow processing time between blocks.

The incoming data is processed through a 4θ conversion block to collapse the QPSK modulation down to a tone. The data out of the 4θ conversion block is processed through one of two paths depending on the mode of operation. At start-up the module will be in acquisition mode until the bulk frequency offset measurement is within the tracking bandwidth of the frequency tracking loop. Once that process is complete, the module will operate in tracking mode.

The data output from the 4θ conversion block in this module is output from this module for use in the Carrier Phase Recovery (CPR) module.

Carrier Phase Recovery

Carrier Phase Recovery (CPR) may use a feed-forward algorithm utilizing a Block Phase Estimator (BPE) and a phase rotation function to remove residual frequency and phase errors. CPR module operates on the on-time data samples produced by the PMD compensation module. The top level carrier phase recovery module diagram is shown in Figure 10.

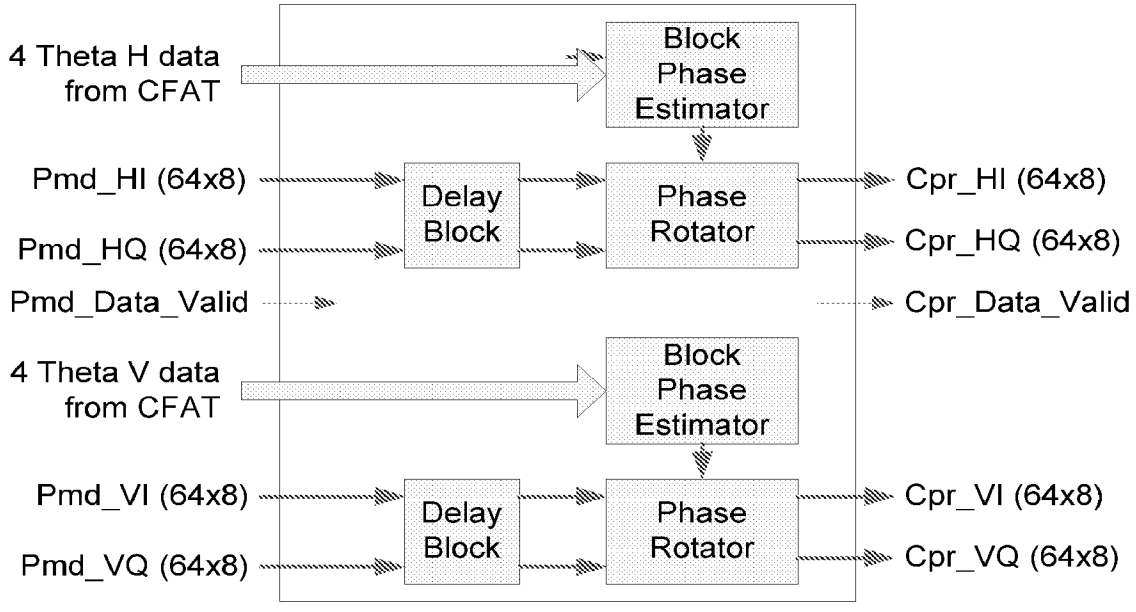


Figure 10: Carrier Phase Recovery Top Level

The on-time data from both polarizations is input and processed through independent, identical processing paths. CPR also needs the I/Q data pairs per polarization to be collapsed to a tone. A similar 4θ conversion occurs in the CFAT module. So the 4θ data is output from CFAT and input to this block thus eliminating the 4θ conversion from this module.

The 4θ data is processed through a BPE to track the phase offsets. The window size of the BPE will be configurable over a small set of fixed values. Within each window, a phase is estimated based on all the 4θ data symbols. The estimation window slides half window size at a time.

The on-time data is also delayed through a delay block to align each symbol in the center of the BPE window.

The delayed data and phase correction value out of the BPE are input to a phase rotator that rotates each symbol by the phase correction value.

Differential Decoder

The Differential Decoder (DDI) module is responsible for accepting symbol streams from the CPR (at 1 sample per symbol) and generating a hard-decision output data stream for the FEC Frame Synchronizer (FFS) module.

In DQPSK mode the incoming data is differentially decoded inside the DDI module and the resulting hard-decision output is sent out to the FFS module.

In QPSK mode the differential decoding is bypassed and just the soft-decision or hard-decision (based on just the sign-bit of the incoming symbol data) is sent out to the FFS module.

The top level block diagram of DDI module is shown in Figure 11.

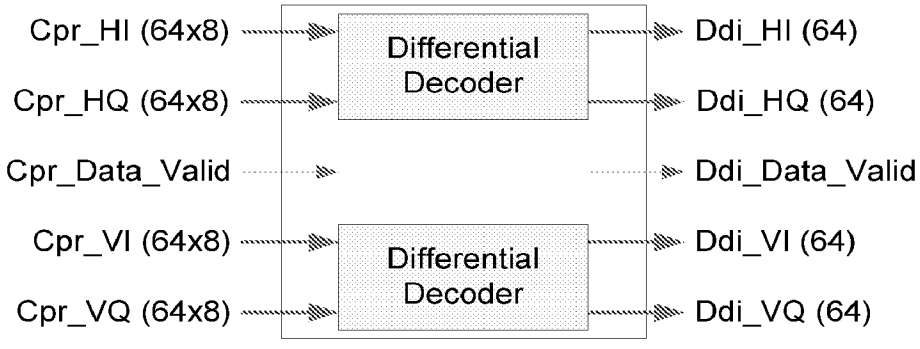


Figure 11: Differential Decoder Top Level

In DQPSK mode DDI uses two consecutive data symbols within the same polarization to figure out the most likely transition which determines the hard-decision information that needs to be sent out to the HDFEC Decoder.

In DQPSK multiple basic pre-coder options may be supported to cover for any transmit and receive implementation mismatches.

Similar flexibility may be provided for QPSK as well where the 2C sign bit of the symbol can be the same as the data bit or the inverse of the data bit.

FEC Frame Synchronizer & FEC Interface

The FEC Frame Synchronizer (FFS) module will help in achieving frame synchronization. The module will consist of three major blocks as shown in Figure 12.

The Data Alignment block may allow several degrees of freedom for skewing, swapping and rotating the channels with respect to each other to help align the channels correctly for the Frame Sync Detection module in the FFS or in an external device be able to decode the channels correctly.

The Frame Sync Detection module in the FFS may implements a hard-decision or soft-decision correlation algorithm with synchronization state machine to search for and synchronize to a known pattern / Unique Word (UW). This module detects and synchronizes to the UWs on both polarizations and helps realign the data stream according to the transmitted order after the UWs have been correctly detected. Note that in mode where UW is not present this module may rely on feedback from an external device that is capable of providing feedback signals to help the Data Alignment block tweak the alignment between the channels till correct synchronization is achieved.

The Clock Transfer module may be responsible for taking the parallel data bus at the internal core clock to a different format bus at a clock speed suitable for the Decoder / Deframer following the DSP.

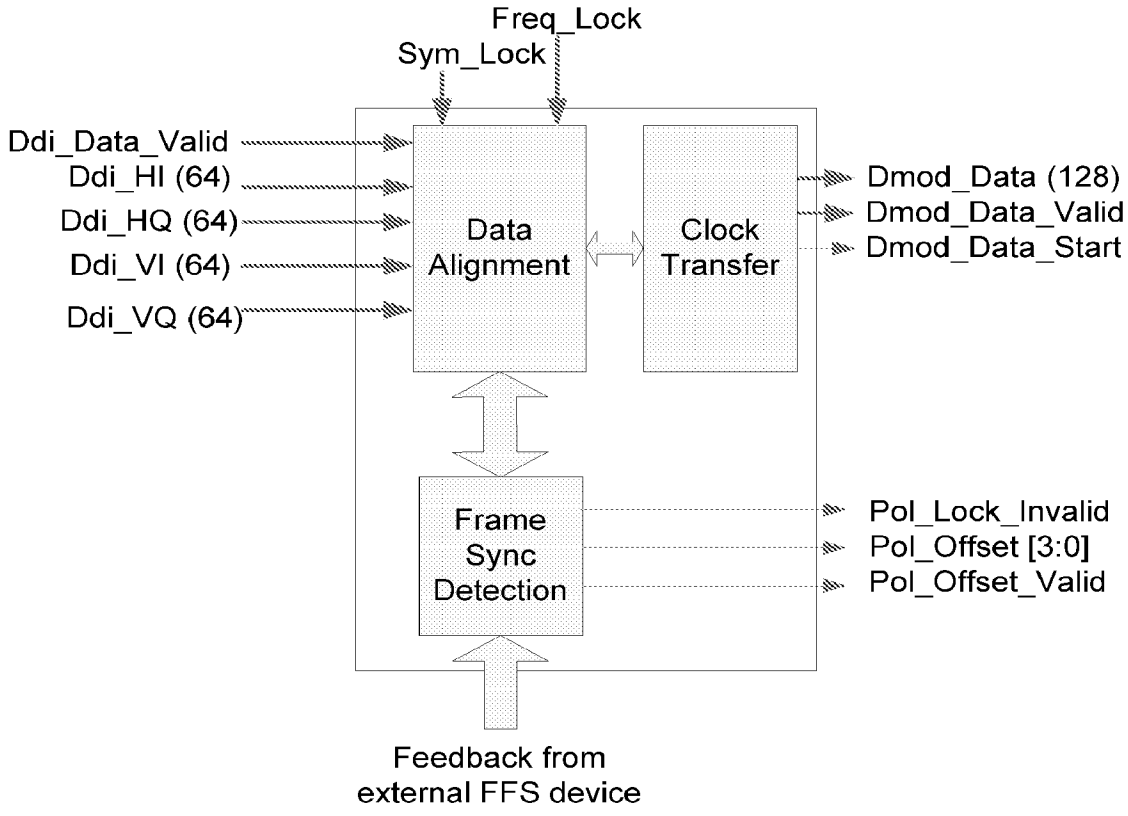


Figure 12: FEC Frame Synchronizer and FEC Interface Top Level

Hard or soft correlation may be used to correlate the incoming complex samples in each polarization with the expected complex UW pattern. The correlation results are compared to a programmable threshold to decide if UW is detected. In DQPSK mode there is no need to solve the IQ phase ambiguity within each polarization. Only in-phase correlation (I to I, Q to Q) is required. And the correlation peak will always be positive.

In QPSK mode this module will resolve the phase ambiguity at every UW.

Soft-input generation for soft-decision FEC decoding of a differentially encoded signal

Problem Currently in 40 / 100 Gbps OTN (Optical Transport Network) systems hard-decision FEC (Forward Error Correction) schemes are being used.

Also because of high phase noise differential encoding is being applied.

Soft-decision FEC (SDFEC) provides higher performance gains if a good quality soft-input can be generated for the Decoder in presence of differential encoding.

Solution Algorithm for soft-input / LLR generation that preserves the BER-in / BER-out relationship for the SDFEC and is suitable for high speed implementation Simplifications to the algorithm for high-speed implementation

Technical Keywords Soft-decision decoding, differential encoding / decoding, DQPSK, SDFEC

Novel This is a new technique. In 40 / 100 Gbps OTN use of SDFEC is not prevalent. Just generating a soft-input / LLR that preserves the SDFEC performance is a innovation. Applying this at 40 / 100 Gbps with low implementation complexity is another innovation.

Inventors Fan Mo and Sameep Dave

Differential Encoding & Decoding Algorithm

Differential Encoding

The Differential encoding is applied with QPSK modulation separately in horizontal and vertical polarizations. Figure 1 shows the differential encoding method. The red constellation dots, labeled as (DI,DQ), represent the output QPSK symbols from the differential decoder. The transition between the constellation symbols are decided by the input symbols, labeled as (CI, CQ), to the differential encoder.

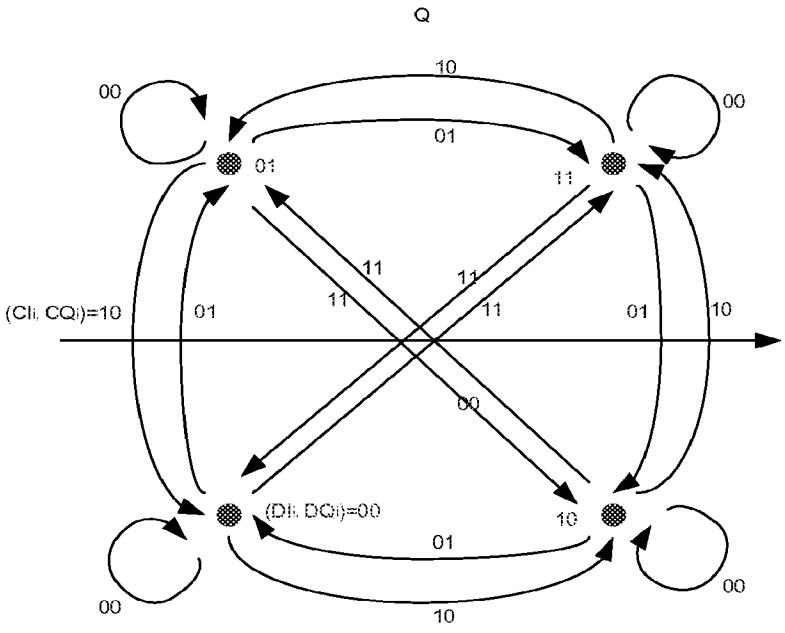


Fig. 1 Differential encoding method

The differential encoder follows the following rules:

Initialization: assume the previous transmitted symbol pattern is 00 so (DI_{-1}, DQ_{-1}) = (-0.707, -0.707)

If the input symbol (CI_0,CQ_0) to the differential decoder at time 0 is

00: no rotation is applied, (DI_0,DQ_0) = (-0.707, -0.707).
01: 90-degree clockwise rotation is applied, (DI_0,DQ_0) = (-0.707, 0.707).
10: 90-degree counter-clockwise rotation is applied, (DI_0,DQ_0) = (0.707, -0.707).
11: 180-degree rotation is applied, (DI_0,DQ_0) = (0.707, 0.707).

Let's assume the pattern for (CI_0,CQ_0) is 10 so (DI_0,DQ_0) = (0.707, -0.707). If the input symbol (CI_1,CQ_1) to the differential decoder is

00: no rotation is applied, (DI_1,DQ_1) = (0.707, -0.707).
01: 90-degree clockwise rotation is applied, (DI_1,DQ_1) = (-0.707, -0.707).
10: 90-degree counter-clockwise rotation is applied, (DI_1,DQ_1) = (0.707, 0.707).
11: 180-degree rotation is applied, (DI_1,DQ_1) = (-0.707, 0.707).

And encoding will be performed continuously following this method.

Differential Decoding

The Differential decoding for is performed in each polarization after coherent QPSK detection. The hard decisions of (CI_i, CQ_i) are made based on judging the most likely transition between each pair of received symbols, (DI_{i-1}, DQi_{-1}) and (DI_i, DQ_i) (noise corrupted at the receiver). The Table 1 below summarizes all the hard decision cases.

Table 1 Hard decision decoding

Case index	(DI_{i-1}, DQi_{-1})	(DI_i, DQ_i)	(CI_i, CQ_i)
0	00	00	00
1	00	01	01
2	00	10	10
3	00	11	11
4	01	00	01
5	01	01	11
6	01	10	00
7	01	11	10
8	10	00	10
9	10	01	00
10	10	10	11
11	10	11	01
12	11	00	11
13	11	01	10
14	11	10	01
15	11	11	00

To achieve the best performance from the down stream SDFEC decoder, we have to also generate the soft input information that represents the reliability of each bit. The ideal method to generate the soft input is to generate maximum-likelihood ratio (LLR) as the input to the decoder. The general Equation for LLR is:

$$LLR_{b_{i_1}} = \frac{\sum P(b_i = 1)}{\sum P(b_i = 0)} \qquad (1)$$

For instance for the bit CI_i, cases 2 3, 5,7, 8, 10, 12 and 13 in Table 1 are corresponding to a hard decision of $CI_i = 1$ and the rest of the cases are corresponding to hard decision of $CI_i = 0$. So the

$$LLR_{CI_i} = \frac{P(00,10) + P(00,11) + P(01,01) + P(01,11) + P(10,00) + P(10,10) + P(11,00) + P(11,01)}{P(00,00) + P(00,01) + P(01,00) + P(01,10) + P)(10,01) + P(10,11) + P(11,10) + P(11,11)} \qquad (2)$$

Here P((DI_{i-1}, DQi_{-1}), (DI_i, DQi)) represent the probability of transition from (DI_{i-1}, DQ_{i-1}) to (DI_i, DQ_i). A total of 16 terms are involved here in the computation so the computational complexity is extremely high. One way to avoid all the real time

computations is to is to use pre computed look-up tables (LUTs). However for high speed designs we have large number of parallel path which will make the LUTs too large to implement. Therefore a simplified algorithm is defined here. Simulations have proved that this simplified method provides insignificant performance degradation compared to using optimal LLRs.

The key for the simplified algorithm is to identify the dominating terms in computing the LLR. The following set of figures in Fig. 2 helps to identify the terms. The blue dots represent (DI_{i-1}, DQ_{i-1}) and the red dots represent (DI_i, DQ_i). To help identify the cases we assume (DI_{i-1}, DQ_{i-1}) is always in the third quadrant, and (DI_i, DQ_i) is moving from 1st quadrant to 4th quadrant in each row. In row 1, DI_{i-1} has the smallest magnitude for cases A to D. In row 2, DQ_{i-1} has the smallest magnitude for cases E to H. In row three, DQ_i has the smallest magnitude in the first quadrant for case I and the red dot is rotated by 90, 180 and 270 degrees for case J to L. In row 4, DI_i has the smallest magnitude in the first quadrant for case I and the red dot is rotated by 90, 180 and 270 degrees for case N to P. All these 16 cases combined cover all relative magnitude possibilities with (DI_{i-1}, DQ_{i-1}) in the 3rd quadrant. By examine the cases we find out for each case what is the most likely transition (represented by (CI_i, CQ_i)) and what is the second likely transition. These two transitions are then used to help us to decide how the LLR information for (CI_i, CQ_i) shall be collected.

For example, for case A, the most likely transition is (CI_i, CQ_i) =11 (transition from (DI_{i-1}, DQi_{-1})=00 to (DI_i, DQi) = 11). Since DI_{i-1} has the smallest magnitude among all, the second most likely transition is (CI_i, CQ_i) =10 (from (DI_{i-1}, DQ_{i-1}) =10 to (DI_i, DQi) = 11 with DI_{i-1} flipped sign). The reliabilities of (CI_i, CQ_i) are decided by both (DI_{i-1}, DQ_{i-1}) and (DI_i, DQ_i). G operation, which computes the joint reliability of two reliability values, is used to calculate the reliability of CI_i and CQ_i. In this case the G operation between (DI_{i-1}, DI_i) should be assigned to CQ_i as the reliability information. This is intuitive since that the flip of CQ_i is most likely event. On the other hand, the G operation between (DQ_{i-1}, DQ_i) should be assigned to CI_i as the reliability information.

In another example of case B, the most likely transition is (CI_i, CQ_i) =01 (transition from (DI_{i-1}, DQi_{-1})=00 to (DI_i, DQi) = 01). Since DI_{i-1} has the smallest magnitude among all, the second most likely transition is (CI_i, CQ_i) =11 (from (DI_{i-1}, DQ_{i-1}) =10 to (DI_i, DQi) = 01 with DI_{i-1} flipped sign). In this case the G operation between (DI_{i-1}, DI_i) should be assigned to CI_i as the reliability information since the flip of CI_i is most likely event. On the other hand, the G operation between (DQ_{i-1}, DQ_i) should be assigned to CQ_i as the reliability information.

By analyzing all 16 cases, we found that 4 of the cases: A, C, E and G shall have the G operation between (DI_{i-1}, DI_i) assigned to CQ_i and the G operation between (DQ_{i-1}, DQ_i) assigned to CI_i while in all other cases, the G operation between (DI_{i-1}, DI_i) should be assigned to CI_i and the G operation between (DQ_{i-1}, DQ_i) should be assigned to CQ_i, we summarized these cases in Table 2.

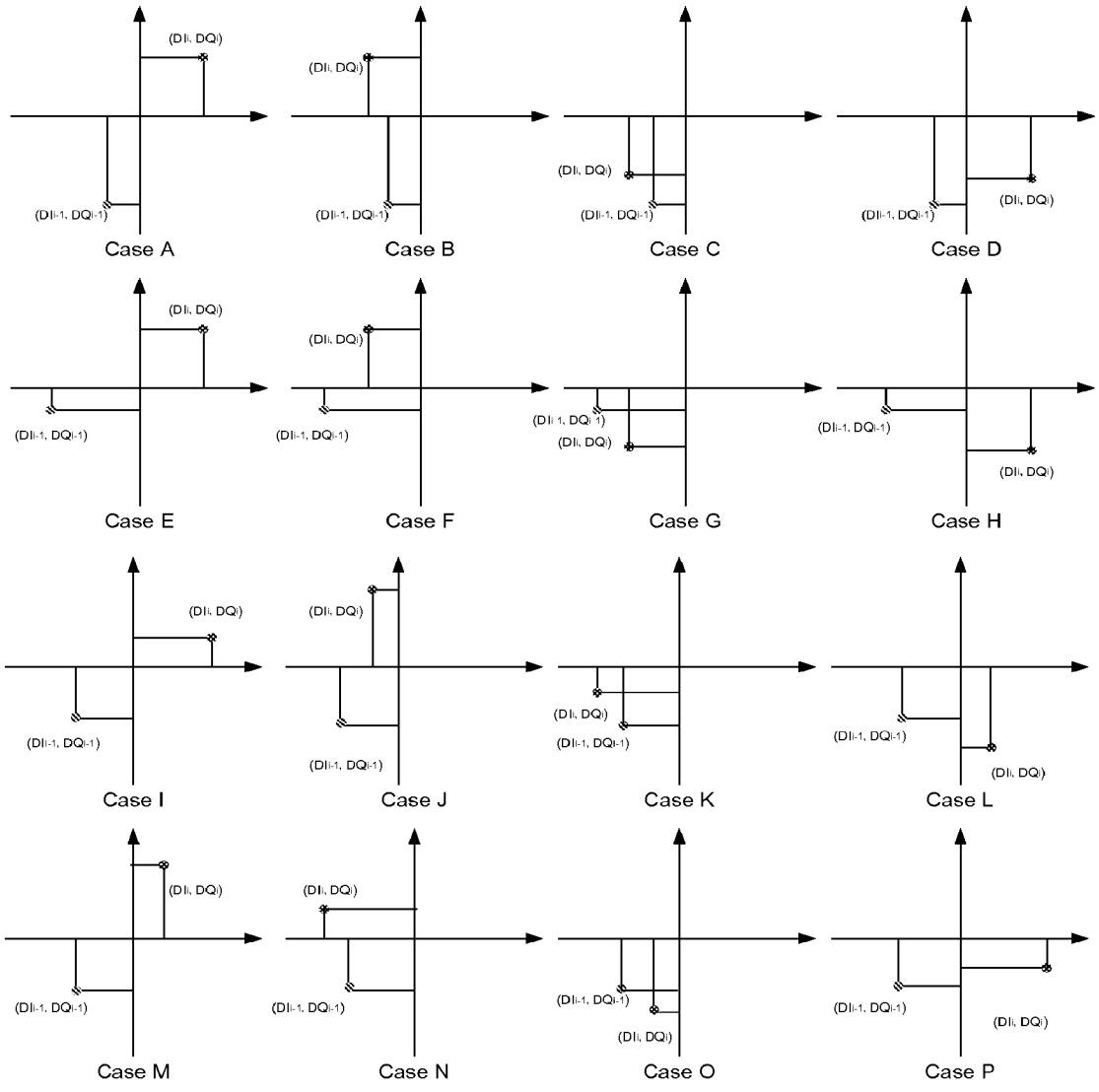


Figure 2: Diff decoding case analysis

Table 2 Reliability assignment for Diff decoder

Case index	Most likely transition (DI_i, DQ_i)	Second most likely transition (DI_i, DQ_i)	Reliability assignment CI_i	Reliability assignment CQ_i
A	11	10	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$
B	01	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
C	00	01	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$
D	10	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
E	11	01	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$

F	01	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
G	00	10	$G(DQ_{i-1}, DQ_i)$	$G(DI_{i-1}, DI_i)$
H	10	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
I	10	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
J	01	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
K	00	01	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
L	10	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
M	11	01	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
N	01	00	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
O	00	10	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$
P	10	11	$G(DI_{i-1}, DI_i)$	$G(DQ_{i-1}, DQ_i)$

The above analysis covers only the cases when (DI_{i-1}, DQ_{i-1}) is in the third quadrant. All other cases with (DI_{i-1}, DQ_{i-1}) in other quadrant are also analyzed.

CDSLLDFT method for tuning very large frequency offsets in 40 / 100 Gbps OTN

Problem Potential for very large starting frequency offset in 40 / 100 Gbps OTN (Optical Transport Network) systems.

Generating error signals to help tune the LO to bring the signal to baseband.

Solution Algorithm for detecting the presence of large frequency offset and providing correction direction / value for appropriate tuning

Reusing frequency bins from the frequency domain CD compensation circuitry
Technical Keywords LO Tuning, LASER tuning, frequency offset

Novel This is a new technique. In 40 / 100 Gbps OTN systems the Rx LO can be way off (several GHz). The invention is a low implementation complexity solution to help achieve lock.

Inventors Matt Nimon, Fan Mo, Bill Thesling and Sameep Dave

Coarse Frequency Estimation

The demodulator may need to operate with large frequency offsets (larger than the symbol rate). The CFAT module is capable of acquiring the input signal in presence of frequency offsets up to ±12.5% of the symbol rate. The FFT capability of the CDC module is used to provide a coarse indication of frequency offset to help bring down the frequency uncertainty to within the ±12.5% range. This is accomplished as described below.

Four samples are taken at the output of the FFT, the FFT bins selected will be programmable through the ACT interface. These 4 samples are referred to in what follows as samples A, B, C, and D, respectively. These 4 samples will be taken and processed every frame (clock).

The magnitude (radius) of each of these 4 samples is computed using the CORDIC common module. Those 4 computed magnitudes are called |A|, |B|, |C|, and |D|, and they are each represented by 9 bits. Each of these magnitudes are filtered via a first order IIR filter transfer function H(z), with programmable alpha, as shown below.

$$H(z) = \frac{alpha}{1-(1-alpha)z^{-1}}$$

The filtered quantities f(|A|), f(|B|), f(|C|), and f(|D|) are then combined algebraically to form the frequency metric as: f(|A|) + f(|B|) - f(|C|) - f(|D|) represented by 11 bits.

The output is brought to the ACT interface where it can be read as a read only status register.

In addition, the filtered quantities are input to a decision block that determines if the frequency offset is high or low. In this block the value: max(f(|A|), f(|B|), f(|C|), f(|D|)) – {(f(|A|)+ f(|B|) + f(|C|) + fl(D|))/4} is computed. If this value less than an programmable input threshold then one of two interrupts (irq_coarse_freq_offset_hi or irq_coarse_freq_offset_lo) is triggered based on the sign of f(|A|) + f(|B|) - f(|C|) - f(|D|) .

The following block diagram provides the low level details:

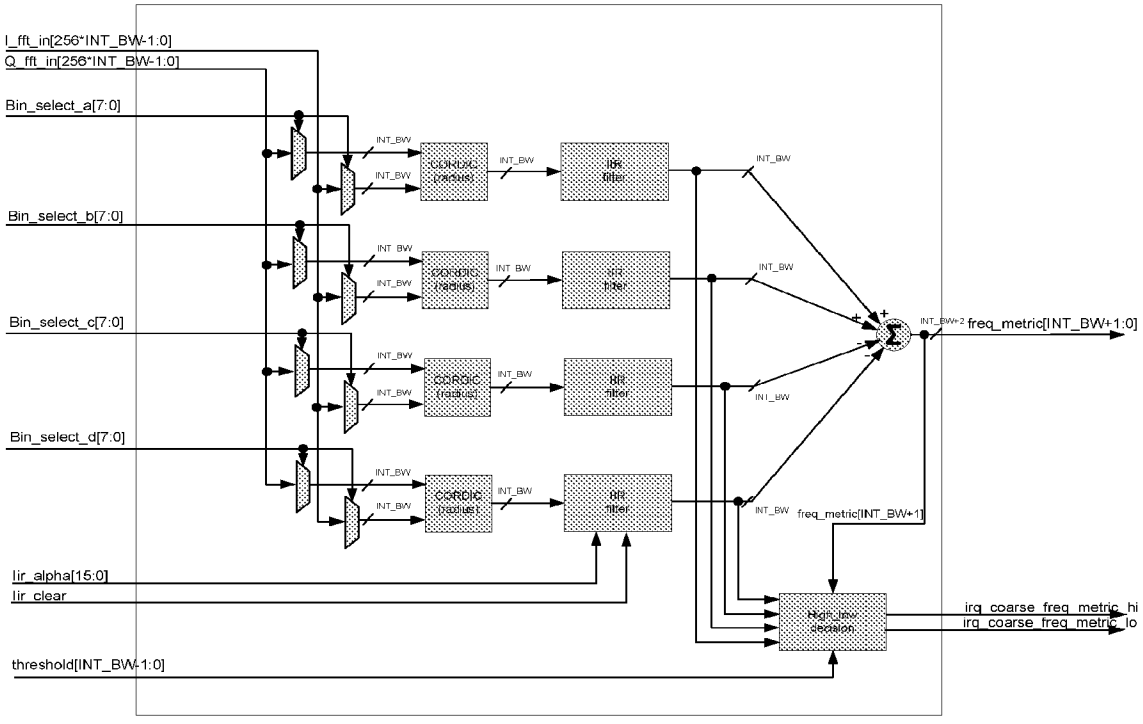


Figure 1. Coarse frequency estimation metric block diagram

Adaptive PMD Equalizer and Implementation

Problem In 40 / 100 Gbps OTN (Optical Transport Network) systems dual-pole transmission is used.

Optical fiber imperfections result in signals interfering across poles. This phenomenon is termed as PMD (polarization mode dispersion)

This interference can change over time and needs to be tracked out

PMD if note recovered can greatly affect the receiver performance

Solution Algorithm for tracking PMD using a CMA based Equalizer that works across both poles
Dual modes for error signal generation
Real and complex incarnations of the Equalizer
Equalizer partitioning for ASIC implementation

Technical Keywords PMD, Equalizer, PM-QPSK, PM-DQPSK, 40 / 100 Gbps, OTN

Novel This is a new approach for tackling PMD. One of the biggest complexity contributors to the receiver design. We have looked at a variety of approaches to make it more manageable for ASIC implementation.

Inventors Fan Mo, Sameep Dave, and Lawrence Esker

Adaptive PMD Equalizer and Implementation

The PMD/PDL compensation module utilizes adaptive equalization / equalizer (EQ) to compensate for PMD (a type of cross polarization interference), PDL (varying received signal strength between poles), and miscellaneous residual impairments that translate into interference / undesired interaction between samples of the same channel / stream / tributary (I or Q samples in a pole. So in DPQPSK transmission we have 2 channels per pole and 4 channels total), or samples of the other channel in the same pole, or samples of other channels across both poles.

The PMD/PDL compensation module takes in data at 2 samples/symbol from the MFD (Matched Filter Decimator) module and processes the data through a bank of FIR filters with adaptive filter taps / coefficients. The filtered output is sent to the STAT (Symbol Timing Acquisition and Tracking), CFAT (Carrier Frequency Acquisition and Tracking) and CPR (Carrier Phase Recovery) modules. STAT gets 2 samples (on-time and off-time) per symbol for half of the symbols (32 contiguous on-time and off-time symbols per valid clock) while CFAT and CPR get 1 sample (on-time) per symbol for all the symbols (64 contiguous on-time symbols per valid clock). The top level block diagram for this module is shown in Figure 6.

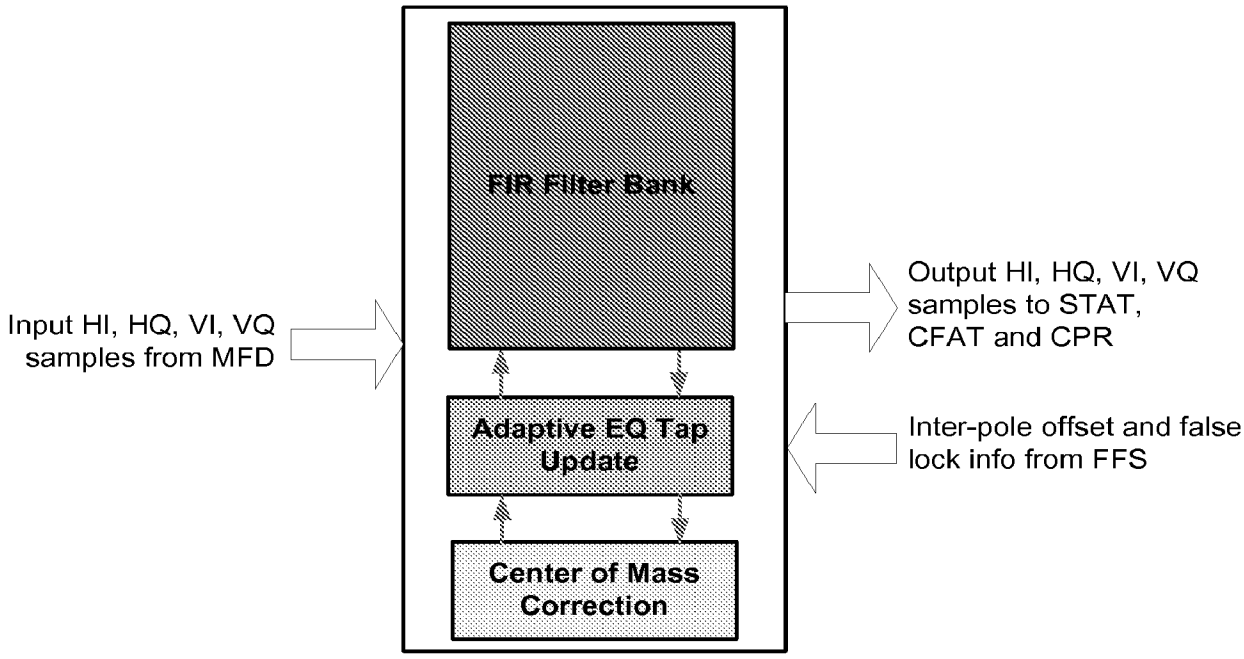


Figure 13: PMD/PDL Compensation module Top Level

The FIR filter bank shown in Figure 6 consists of sixteen, 16-tap real FIR filters operating at 2 taps per symbol. A conceptual view of the filter bank is shown in Figure 7.

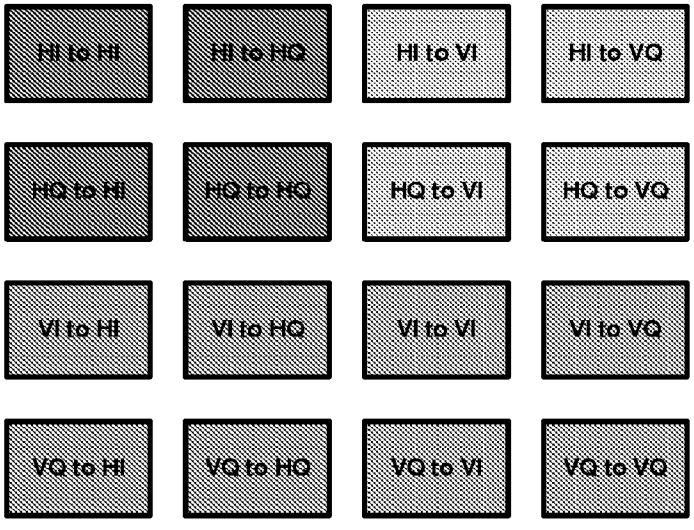


Figure 14: PMD/PDL Compensation module Filter Bank

Each box in Figure 7 represents a 16-tap FIR Filter. The boxes are marked to indicate that they are responsible to cover the impact of which input channel to which output channel. For example the HI to VQ box means the filter is calculating the impact of HI (Horizontal-pole In-phase signal) on to VQ (Vertical-pole Quadrature-phase signal). So every row in the Figure 7 represents the impact of a certain input channel on every output channel. And every column represents the impact of all input channels onto a particular output channel. (1) shows the math behind the HI output generated by the first column in Figure 7 :

$$Out_{HI,n} = \sum_{i=-7}^{8} \left(In_{HI,n+i} \times T_{HI2HI,i} + In_{HQ,n+i} \times T_{HQ2HI,i} + In_{VI,n+i} \times T_{VI2HI,i} + In_{VQ,n+i} \times T_{VQ2HI,i} \right) \quad (1)$$

Where

n is the sample index (lower number is earlier in time),

i is index variable,

Out is the output sample where the first subscript shows the output channel and second subscript is the sample index,

In is the input sample where the first subscript shows the input channel and second subscript is the sample index,

and T is the set of filter taps where the first subscript shows which of the 16 filters (have use *2* notation instead of * to *) and the second subscript is the tap index assuming a 16-tap filter where index 0 is the center tap. Please note that for C or RTL indexing the taps may be numbered from 0 to 15 with 7 being the center tap. As longs as the indexing is consistent in terms of functionality we will be in good shape.

Midway through the system design and simulations it was decided that for some applications of PMD/PDL compensation module we will use complex FIR filters. What this translates into is that each quadrant (same color boxes) in Figure 7 is a complex filter instead of the four real filters shown. The complex filter decision took one degree of freedom away and so now within a quadrant the filters that are diagonally across to each other have the same taps or taps that are opposite in sign. Figure 15 shows the interdependence of the taps in case of complex filtering. The taps for filters connected by the black line (negative slope diagonal) are the same while the taps for filters connected by the red line (positive slope diagonal) are opposite in sign.

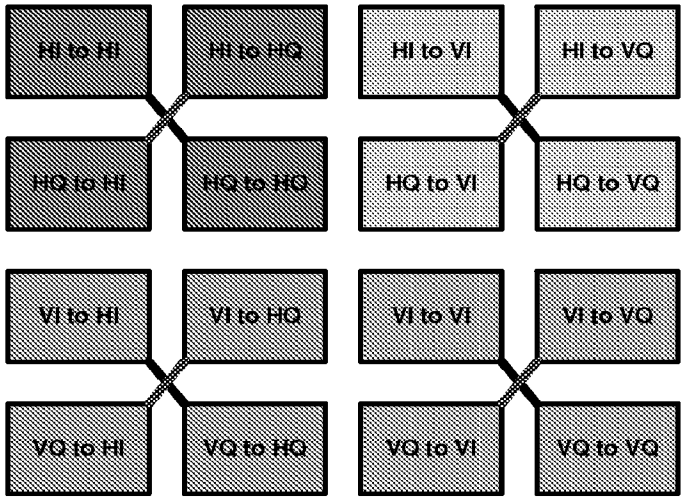


Figure 15: PMD/PDL Compensation module complex FIR filter bank

For the filter tap updates on POLO CMA (Constant Modulus Algorithm) is used. CMA drives the on-time (at optimal symbol timing) constellation points on each polarization to a circle with a desired radius with minimum radius variation. The filter taps are usually initialized as an all-pass filter with only the center taps $T_{HI2HI,0}$, $T_{HQ2HQ,0}$, $T_{VI2VI,0}$ and $T_{VQ2VQ,0}$ initialized to unity while rest of the taps are all zeroes. And using only on-time output samples the filter taps are updated using an error signal as shown in (2) or optionally a simpler mechanism shown in (3).

$$T_{HI2HI,i,n} = T_{HI2HI,i,n-1} + (\beta - (Out_{HI,n}^2 + Out_{HQ,n}^2)) \times Out_{HI,n} \times In_{HI,n+i} \times \mu) \quad (2)$$

$$T_{HI2HI,i,n} = T_{HI2HI,i,n-1} + sign(\beta - (Out_{HI,n}^2 + Out_{HQ,n}^2)) \times Out_{HI,n} \times In_{HI,n+i} \times \mu) \quad (3)$$

Where

Out^2 is the squared on-time output sample where the first subscript shows the output channel and second subscript is the sample index,

β is desired threshold (squared radius) which CMA is driving towards,

μ is a gain factor that affects the speed and stability of CMA's convergence,

sign(.) is just calculating the sign of the operand,

and rest of the variables have the same meaning as in (1).

The adaptive EQ receives a few feedback signals from the FFS (FEC Frame Synchronizer) module. In certain fiber channel conditions the filter taps can converge such that the outputs on both poles is the same (both are locked to H or both are locked to V). In such cases the FFS indicates that the polarization lock is invalid and EQ will reinitialize the taps (to their default value as configured via the APB interface) that generate the Vertical pole (filters in the right half of Figure 15). This re-initialization

should result in the EQ converging on different poles. This process can be performed recursively till the desired convergence is achieved.

Also at initial acquisition stage if the FFS detects a timing offset between the two poles it will convey that offset value to the EQ so that the filter taps can be re-initialized or shifted to compensate for the offset. This offset is performed in a balanced fashion between the filter taps generating the outputs for the two poles to make sure sufficient taps are available towards the edge of the filter. If such compensation is not performed the EQ might converge such that during normal operation the higher weight taps (on one of the poles at any time) get skewed towards the edge of the filter essentially turning the EQ into a filter with small number of useful (relatively bigger value) taps.

The EQ is also a part of the symbol timing loop along with the STAT module. The EQ can interact with the symbol timing loop in such a fashion that at times the EQ filter taps on both poles can start drifting towards the edge of the filter, again turning the EQ into a filter with small number of useful taps. CoM evaluation and correction will be performed in the PMD / PDL compensation module to make sure that if the useful EQ taps have shifted by a symbol they are moved back towards the center of the filter. To figure out if the taps have moved the CoM will be calculated as the difference between the combined tap energies of the filter taps index -7 to -1 and filter taps index 1 to 7. If the magnitude of this difference is greater than a programmable threshold the taps are instantaneously adjusted towards the center. Please note that adjustment of taps will result in addition or deletion of a symbol and needs to be accompanied by the deletion or addition (respectively) of a symbol in the data going out (to CPR and CFAT).

A combination of the FIR filter bank, the CMA update algorithm and tap / output adjustments based on CoM and feedback from FFS will lead to a stable and powerful PMD / PDL compensation design.

I/Q Skew compensation / tracking in 40 / 100 Gbps OTN

Problem Small I versus Q timing skew / offset can cause huge performance degradation in 40 / 100 Gbps OTN (Optical Transport Network) systems.

Evaluating the I versus Q skew in the presence of various optical impairments is very challenging.

This skew can vary over time / temperature and needs to be tracked.

Solution Algorithm for generating a reliable error signal for measuring I versus Q skew in the presence of miscellaneous high speed board design related issues as well as optical impairments like CD, PMD,

Algorithm for removing I versus Q skew at calibration

Low complexity algorithm for tracking and correcting changes in I versus Q skew over time

Technical Keywords I/Q Skew, I versus Q skew, Sampling time offset

Novel This is a new technique. In 40 / 100 Gbps OTN systems very small (several ps) skew between I and Q channels of a QPSK signal is a big fraction of the symbol duration and very detrimental to performance. Generating an error signal that provided basis for correction in presence of all the impairments was very challenging. The techniques to use this error signal at calibration time as well as run-time are also new innovations.

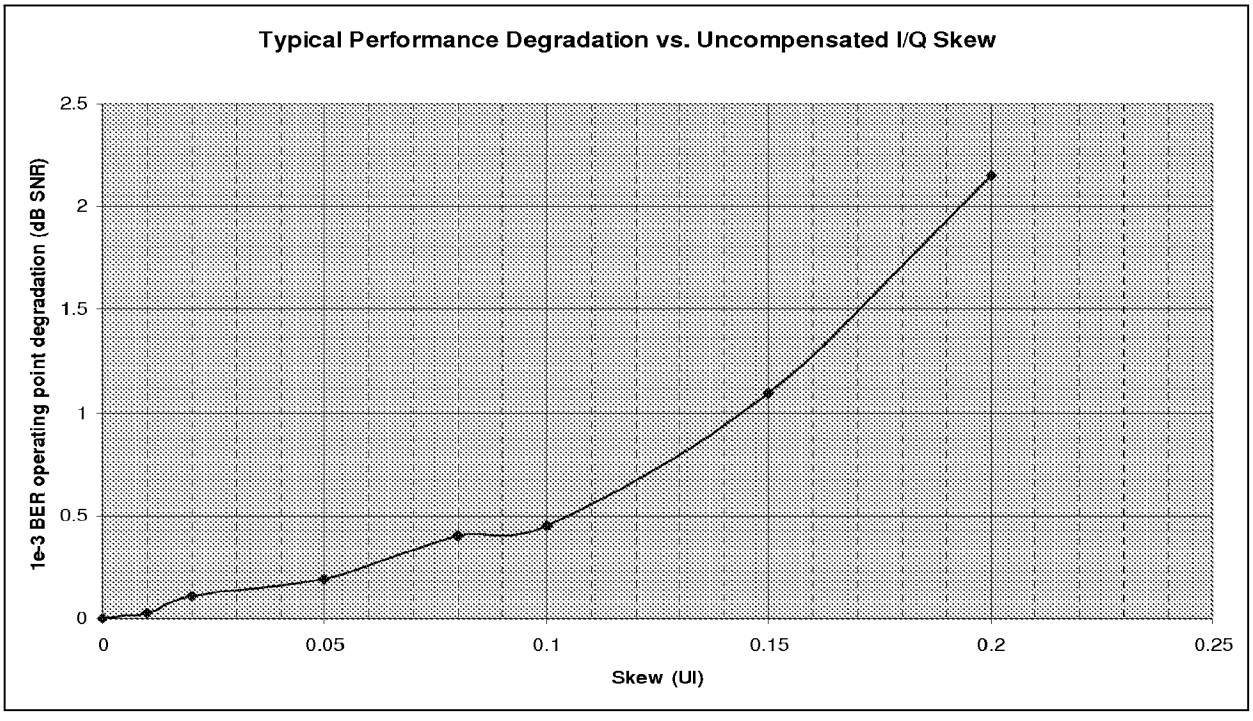
Inventors Yuri Zelensky and Fan Mo

I/Q Skew compensation / tracking in 40 / 100 Gbps OTN

Most current designs for a digital demodulator try to compensate for three types of quadrature demodulator imperfections – DC offset, Amplitude Imbalance and Phase Imbalance. As data rates increase an additional impairment can become an issue – a propagation skew between the I and the Q channel. This impairment behaves differently from the other three and requires a different approach. One way that this was handled in the past was to have an initial skew compensation calibration in the digital domain to calibrate out the imperfections in a given receiver. However, as data rates are increasing, the thermal drift over time can become significant enough in order to merit a real-time adaptive skew-compensation circuit.

If skew is left uncompensated, it can lead to severe degradation in demodulator performance. Below is an example set of simulated performance for a 40Gbps optical demodulator with a comprehensive set of other channel impairments, recording an expected post-demodulator 1e-3 BER SNR operating point in the presence of various

amounts of uncompensated I/Q skew. I/Q skew is measured as a fraction of UI (Unit Interval) or symbol interval, where a symbol interval is two ADC samples:



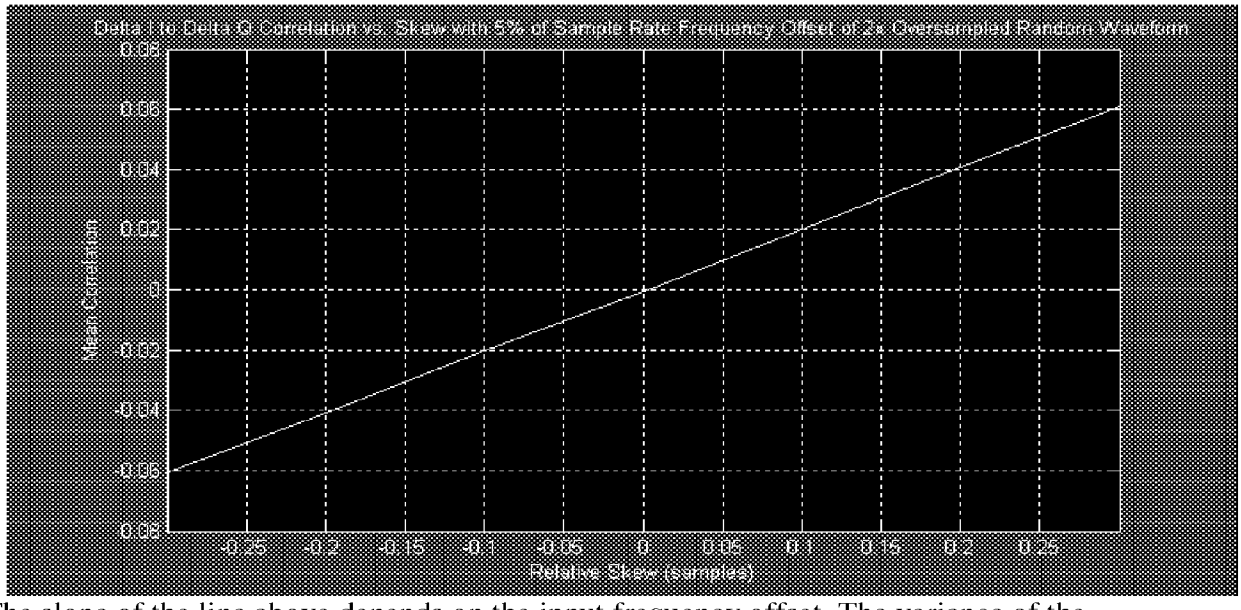
From above, in this particular case a 2% UI skew causes about 0.1dB performance degradation, while a 20% UI skew causes over 2dB of degradation. The total amount of degradation will depend on the relative operating point that is being examined – in this case it is around 11 dB SNR.

Analysis

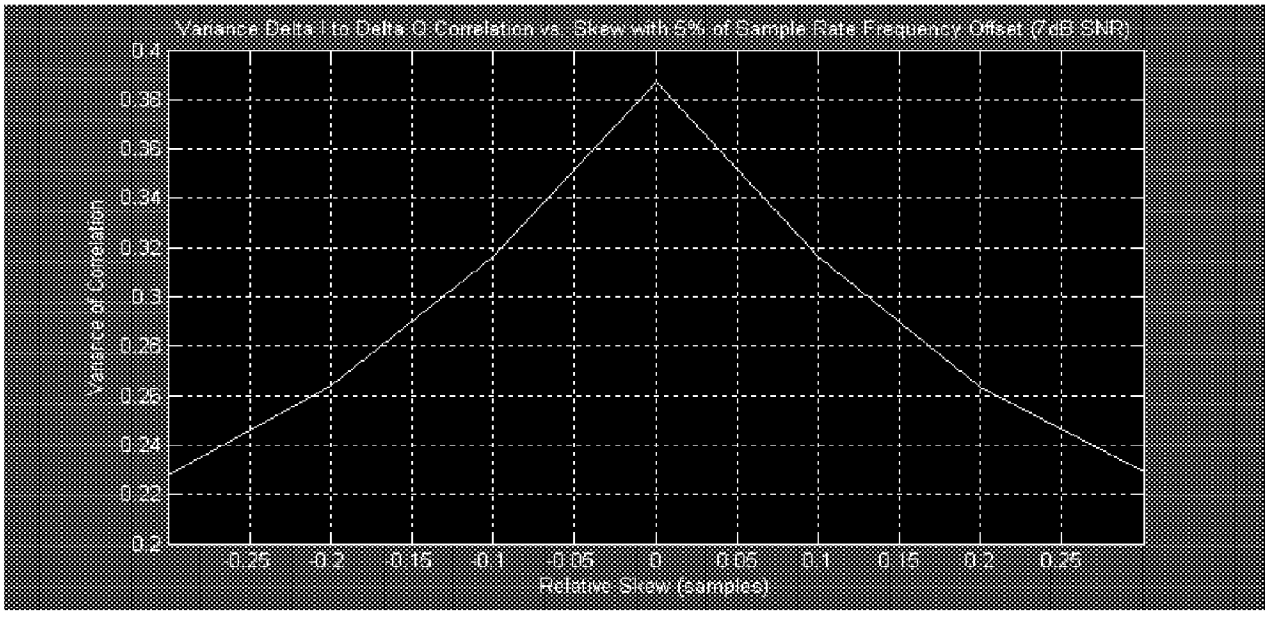
From a practical perspective, our goal is to find some metric of the received ADC samples that indicates if there is a significant amount of timing skew between the two channels. Because we know that skew causes performance and EsNo degradation, the most straight forward way is to demodulate signal with different amounts of up-front skew and pick the skew amount that maximizes receive EsNo. This is a practical approach during initial calibration, but if skew adjustment is required during normal operation this would require either 2 fully-parallel demodulators or a constant performance degradation as different amounts of skew are tried – first case being impractical from demodulator size perspective and second from performance perspective. If the input signal is relatively well behaved (not too many channel impairments) it is possible to perform a signal quality estimation early in the demodulator chain and not need two fully parallel paths – just one main path and a secondary path that tries alternative skew amounts and processes data to a certain extent in order to extract a meaningful quality estimate. Unfortunately, in a high-speed optical channel, impairments such as Chromatic Dispersion, Polarization Mode Distortion and significant carrier

frequency offset need to be compensated prior to being able to properly evaluate the signal quality, making this option still impractical.

It turns out that if there is a certain amount of frequency offset from baseband at the ADC input then a skew between the I and Q paths generate an image signal and the amount of skew can be extracted from a correlation between the I and Q samples. This correlation turns out to be proportional to both skew and frequency offset. Unfortunately, any amount of phase imbalance in the quadrature downconverter also manifests as an I/Q correlation and, in fact, this is how it is normally removed. So it seems we have an additional problem – not only will skew degrade performance, but also, coupled with a significant frequency offset, it will also distort the I/Q phase imbalance compensation. Fortunately, there is another aspect that sets skew plus frequency offset apart from phase offset—in the presence of a time skew and a frequency offset there is a non-zero correlation between first derivatives of the I and Q samples. This correlation is exactly 0 if I and Q correlation is removed, which is typically done by the phase equalizer. This property is independent of the modulated signal, as long as the signal is "normal" and is not centered at baseband. Below is a typical result with a completely random signal, upsampled by 2 and a -7dB AWGN noise added after upsampling and a non-zero frequency offset:

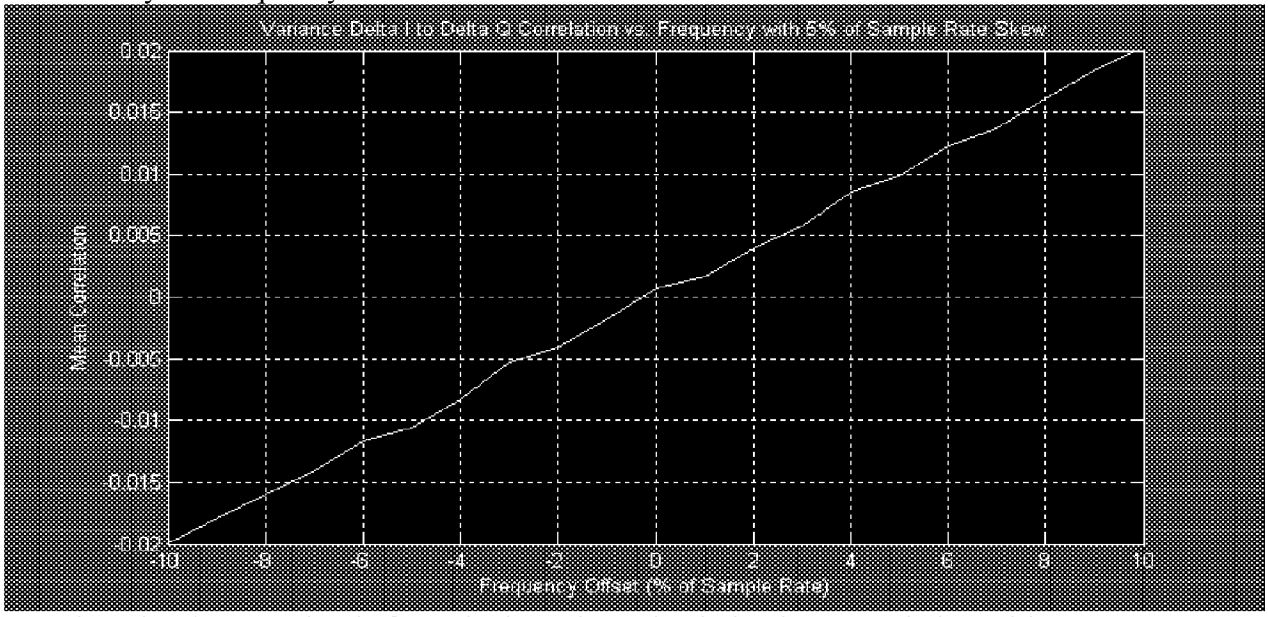


The slope of the line above depends on the input frequency offset. The variance of the samples will help determine how many samples need to be averaged for a statistically significant estimate:



Note that here UI represents one sample period. If we are dealing with a demodulator that processes 2 samples per input symbol, a UI is twice as long.

Now we need to determine what is the smallest frequency offset that we can tolerate and still get a statistically significant estimate of the skew. Let us examine the correlation of I and Q derivatives with just a the same signal, now with a fixed skew of 5% of the sample rate and vary the frequency offset:



Based on the above, a simple formula that relates the derivatives correlation with frequency offset and skew can be derived: C = 4*F*S*P, where:

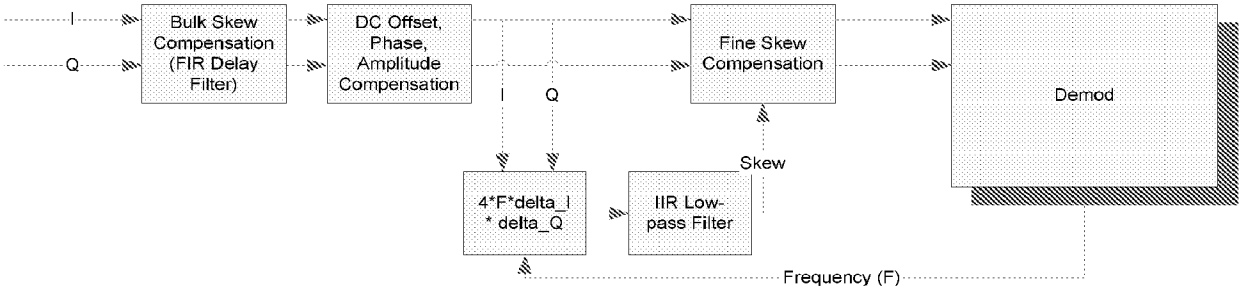
C = average correlation of I and Q derivatives

F = Frequency offset (normalized to sample rate)

S = I to Q time skew (normalized to sample rate)
P = input signal power.
This formula seems to hold true for any 2x oversampled waveform.
This allows us to determine the number of samples that needed to be averaged for a meaningful skew estimation. For example, we have a system that is at 2 samples per symbol and we want to ensure that skew is tracked to 0.5% of a symbol period (or 1% of sample period) and we can ensure that input frequency error will on average be no smaller that 0.5% of the sample rate or 1% of the symbol rate then our mean correlation should be 4*(0.005*2)*0.01=4e-4. With a worst-case of 7dB SNR we can expect worst-case variance on this measurement of 0.5. So if we want the variance of the estimate to be 25% of actual, i.e. 1e-4 then we need to average (1/1e-4)^2=1e8, or about 5 milli-seconds at 20Gsps. If we don't expect the skew to vary by more than 0.005 UI in a second, we can reduce hardware complexity by using one out of every 128 or so samples in order to come up with the estimate.

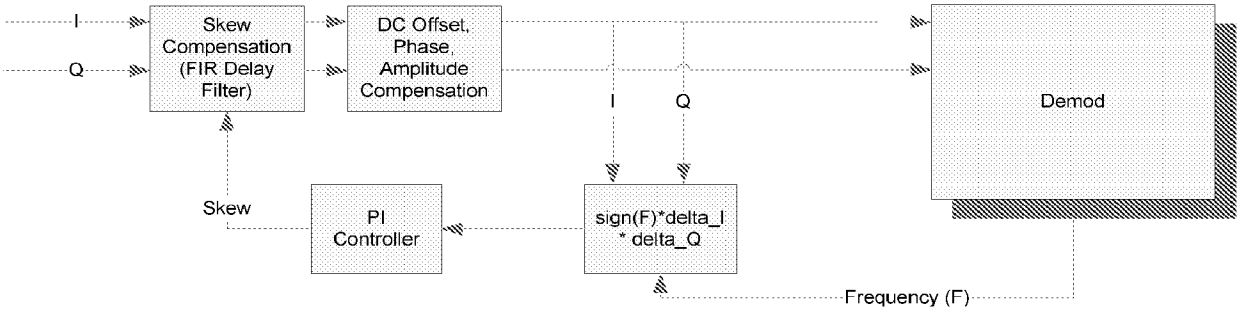
Implementation

Let us now consider several possible HW implementations of a skew compensation filter. Since we know the relationship between skew, frequency and correlation, the most straight-forward implementation is:

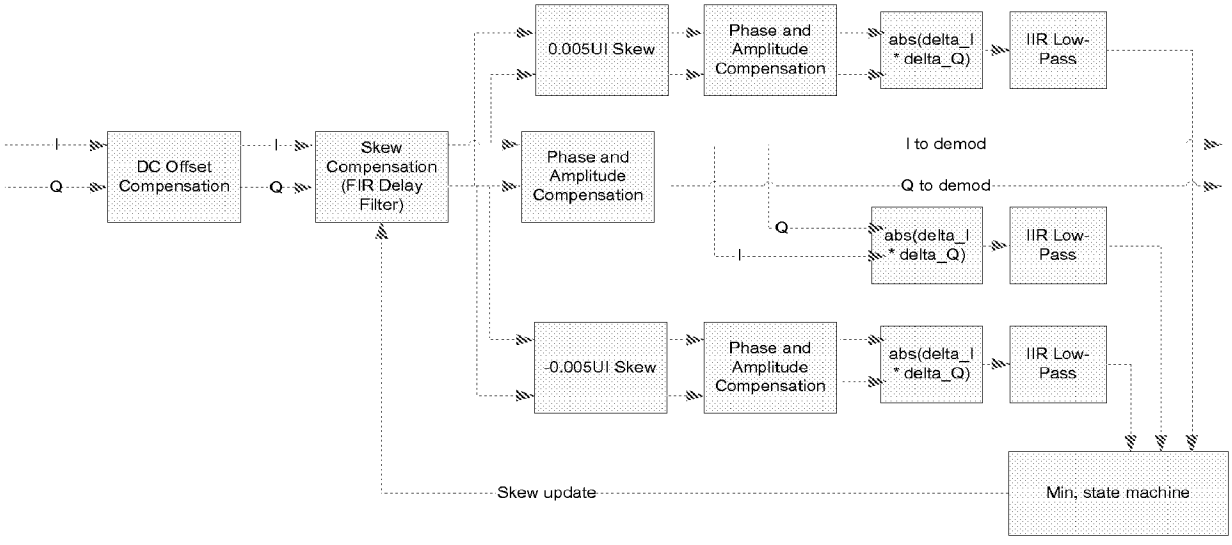


The bulk skew compensation takes out skew that is more than 0.5 UI and has to be configured during calibration. The main drawback of this implementation is that frequency has to be known, so it may be problematic if frequency offset is small and is changing, so that there is some error in the frequency value fed back from the demodulator.

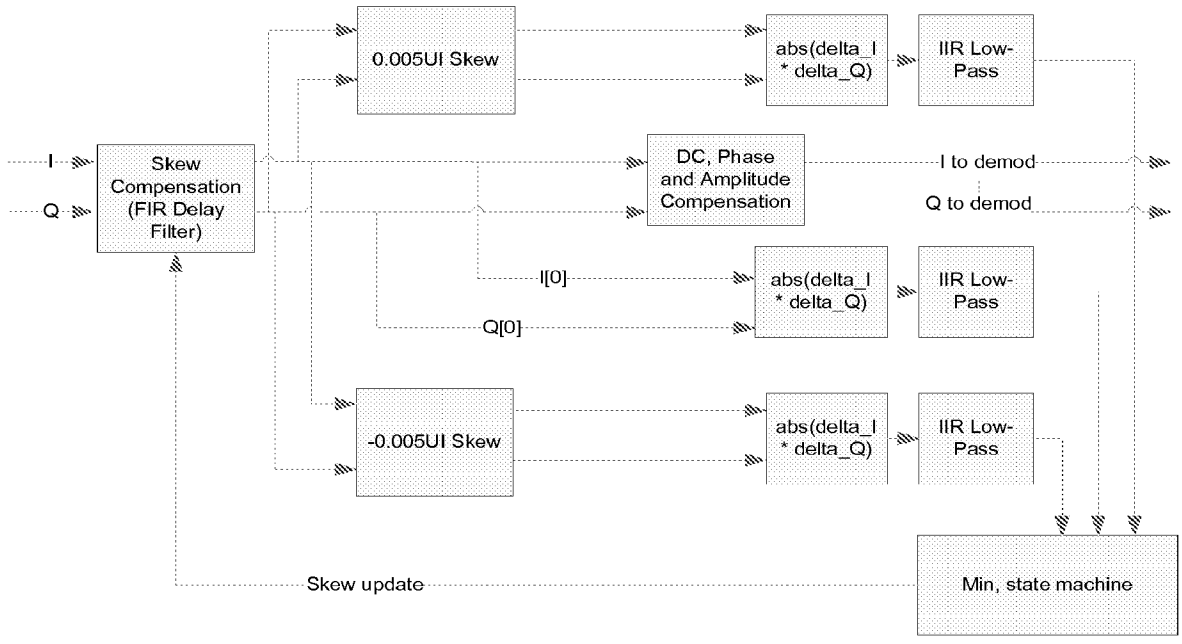
If we can assume that the demodulator is not going to provide an exact frequency value but can at least supply the sign of the frequency error we can do the following:



This implementations uses a slow feedback loop and combines bulk and fine skew compensation in one step. It still relies on some knowledge of the frequency offset. If we can assume no knowledge of frequency offset we can do the following:



In this implementation, we are simply looking for the minimum absolute value of the correlation with trials of a little additional positive and negative skew. The state machine resets the low-pass filters and waits a pre-defined amount, it then compares the three filtered correlation values and if the skewed correlations become smaller than the unskewed correlation it updates the main skew compensation filter and resets the IIR's. Finally, examining the interplay of various compensation filters, it turns out that the delta_I*delta_Q skew metric is not affected by even significant amounts of uncompensated DC, amplitude, or phase error. We can therefore simplify to the following solution:



Once again, as in the previous solution, the delta_I*delta_Q correlators can run on sub-sampled version of the samples, and the state machine updated the main skew compensation block if the center correlation is not smaller than the two +/- trials.

Multi-Layered decoding of concatenated codes

Problem Extracting maximum coding gain from hard-decision or soft-decision iterative decoding of concatenated codes

Reducing the odds of false convergence of decoding algorithms

Solution Algorithm for decoding concatenated codes in a multi-layered fashion where more likely corrections are made first to avoid creating more bit errors during initial iterations

Adapting the algorithm for high speed hard-decision TPC Decoding

Adapting the algorithm for high speed soft-decision TPC Decoding

Technical Keywords Concatenated codes, soft decoding, hard decoding

Novel This is a new technique. Can be used for performance enhancements in a variety of FEC applications.

Inventors Sameep Dave and Fan Mo

Multi-Layered decoding of concatenated codes

Decoding of powerful concatenated codes is usually an iterative process where during every iteration a pass at decoding is performed hich helps generate some extra information about the confidence in a bit being a 1 or a 0. During the initial iterations in the decoding process sometimes the decoder ends up making wrong decisions as the incoming data is very erroneous.

The proposed invention targets making the first few iterations during the decoding process more conservative by limiting the correction capability of the codes involved. This in turn would avoid the initial iterations from making things work. The full correction capacity of the code can then be unleashed on relatively cleaner data for quicker convergence and higher performance.
This technique can be applied to hard decision as well as soft decision concatenated code decoders.

Low complexity interpolator / decimator for 40 / 100 G applications

Problem Sampling rate at the Rx side in OTN systems is usually 2 + delta times the symbol rate

2x or 1x samples per symbol signaling is required for most of the Demodulator design Variable rate interpolators are very complex for 40 / 100 Gbps kind of applications / implementation

Solution Algorithm for generating a compact interpolator / decimator design optimized around the desired sampling rate to symbol rate ratio

Fixed taps filter for lower complexity

Carefully crafted connections to reduce congestion in routing for ASIC / FPGA implementation

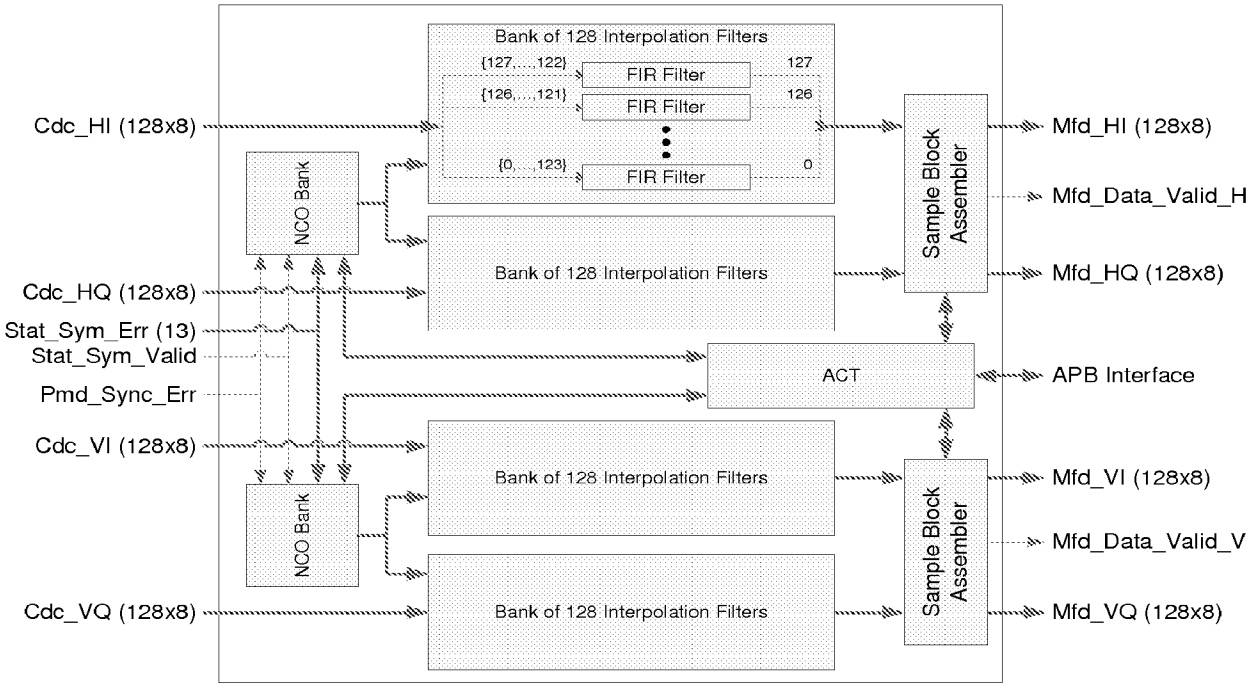
Technical Keywords Interpolator, Decimator

Novel This is a new technique. Can be used for variety of applications where range of desired sampling rate to symbol rate ratio is not huge.

Inventors Matt Nimon, Fan Mo and Bill Thesling

Low complexity interpolator / decimator

The matched filter decimator module implements an interpolation function that provides decimation from the ADC sample rate to 2x the symbol rate. Each of the four data streams has an independent bank of FIR filters with fixed coefficients. The filter coefficients implement a Raised Cosine low-pass filter with pre-determined roll-off. The symbol timing error input value fine tunes the decimation rate such that one of the two samples per symbol output is an on-time sample. The sample block assembler takes in the data samples from the filter bank and groups the samples such that valid data output from the MFD block always contains data samples output per stream. Note that valid output data is not available on each clock and the data valid output indicates when valid output data is available. The top level matched filter decimator design is shown in the figure below.



The MFD supports a single decimation rate. The decimation rate is based on the specification that the ADC sample clock will be set to 2+ times the nominal baud rate and the fact that the MFD outputs 1 or 2 samples per symbol.

Each NCO bank maintains a symbol rate NCO and generates a vector of interpolation phase values per clock. The interpolation phase values are identical for both the I and Q streams in each polarization so one NCO bank services two streams. The Pmd_Sync_Err in an input from the PMD module and is asserted if ever the data valid outputs from both polarizations are out of sync. When the Pmd_Sync_Err is asserted, the NCO banks are cleared.

The symbol error is a signed value providing for a maximum symbol timing correction capability of a certain % of the baud rate. The symbol timing error is input to the NCO bank where it is added to the nominal NCO step value to produce a corrected NCO step. The corrected NCO step value is reported as status.

There are four banks of interpolation filters in the module with each bank processing one of the data streams. Each filter bank takes in one data word of sample data and an array of interpolation phases per clock. The filter blocks filter the incoming data through the filter banks with the interpolation phase for each filter driven by the corresponding interpolation phase value. The filter bank produces 2 samples per symbol out for each data stream.

The decimation rate is controlled by a NCO so the number of output samples produced per clock is not a constant. In order to simplify data processing through the remainder of the demodulator, data samples are gathered and assembled into blocks of samples per

stream per clock by the sample block assembler. The assembly function is identical for the I and Q streams in each polarization so one assembly block services two streams.

As the ratio of the output/input samples per clock is not exact, there will be clock cycles where the matched filter decimator does not output any data. The Mfd_Data_Valid_x output is asserted only on clocks with valid output data. There is one output data valid flag per polarization (we really need only one but two facilitates the division of this function into two HLBs).

CoM based adaptive EQ tap correction

Problem In digital demodulator design adaptive Equalizers are used for recovering signal quality

Equalizer usually plays a part in the symbol timing error correction

In presence of slow residual symbol timing offset the taps of an adaptive equalizer can drift towards the edges degrading the performance

This problem is hastened in the PMD compensation equalizer for 40 / 100 Gbps OTN applications / implementation

Solution Algorithm for generating a CoM (Center of Mass) metric for the equalizer Algorithm for using the CoM metric to correct the taps without disrupting the receiver synchronization

Low complexity implementation of the algorithm for high speed receiver design

Technical Keywords Equalizer, Adaptive filter, CMA, LMS

Novel This is a new technique. Can be used for variety of applications where equalizers are used in the receiver design.

Inventors Fan Mo and Sameep Dave

CoM based adaptive EQ tap correction

In digital Demodulator designs for 40 / 100 Gbps optical systems the PMD compensation Equalizer (PMD EQ) is also a part of the symbol timing loop along with the STAT module. The EQ can interact with the symbol timing loop in such a fashion that at times the EQ filter taps on both poles can start drifting towards the edge of the filter, turning the EQ into a filter with small number of useful taps. This invention proposes CoM evaluation and correction to be performed in the PMD / PDL compensation module to make sure that if the useful EQ taps have shifted by a symbol they are moved back towards the center of the filter. To figure out if the taps have moved the CoM will be calculated as the difference between the combined tap energies of the filter taps index -7 to -1 and filter taps index 1 to 7. If the magnitude of this difference is greater than a programmable threshold the taps are instantaneously adjusted towards the center. Please note that adjustment of taps will result in addition or deletion of a symbol and needs to be accompanied by the deletion or addition (respectively) of a symbol in the data going out of the PMD EQ.

The **pmd_err_com_eval** module performs CoM related Offset and Error Calculation, Tap Offset Control as well as Tap Reset Control as shown in Figure 16. It gets the partial 20-bit CoM metrics (Com_Out_*) from the hlb_pmd_fir 4, 5, 6 and 7 and generates two

outputs that can help counter the movement of EQ filter taps (towards the edges) as shown in Figure 17.

The partial CoM metrics from the HLBs generating outputs for a particular pole are summed together before being weighed by a pole-dependent scaling factor (Z_Com_Gain_*). These gains / weights are to account for any PDL related mismatch between the two poles. The scaled results are added together and this accumulated value is used to generate couple of options for correcting the CoM. A programmable rounding / saturating oprion is made available via the Z_Com_R signal. This dictates how many LSBs versus MSBs are removed when the 12-bit output is generated.

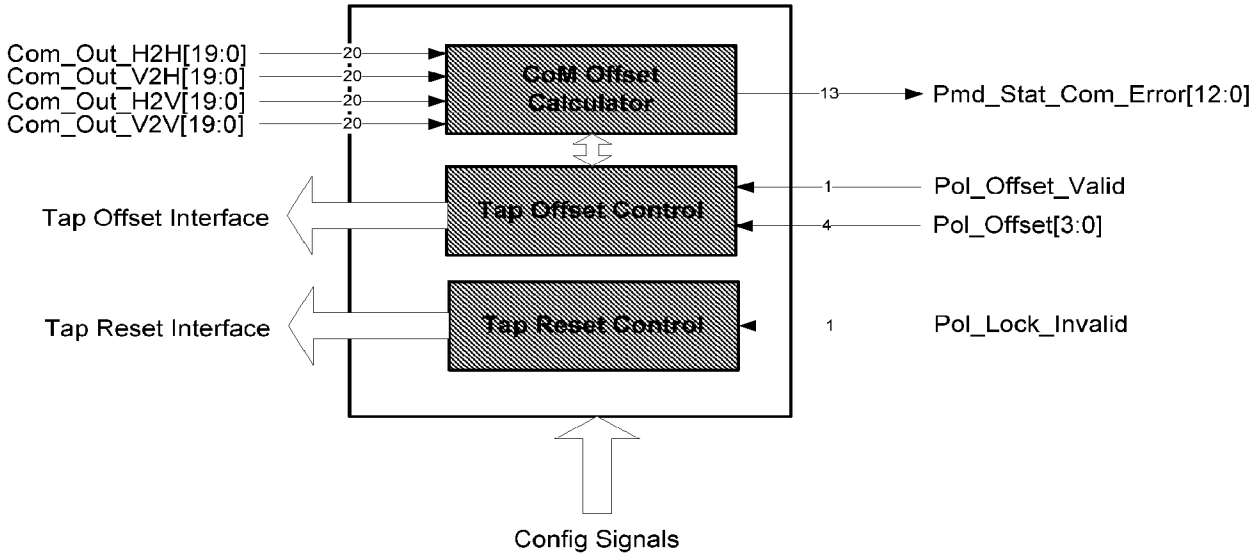


Figure 16. Operations performed by pmd_err_com_eval

The first output (preferred approach) of the CoM Error / Offset Calculator is the error signal Pmd_Stat_Com_Error[12:0] going out to the STAT module. The STAT module can use this signal in addition to its own early-late symbol timing error signal to provide an aggregate error signal to the MFD for symbol timing adjustment.

The second output (2nd option) is a 2-bit offset indicator (Com_Offset[1:0]) that goes out to the Tap Offset Control. This will result in the EQ shifting the filter taps to balance the CoM. The selection between the two options can be performed using the programmable controls shown in Figure 17. Setting the gain Z_Com_Stat_G[7:0] to 0 would turn off the first option. The sign of Z_Com_Stat_G[7:0] can control the polarity of the CoM metric ((early taps – late taps) versus (late taps – early taps)). Setting the Z_Com_Th[11:0] (unsigned) to 0xFFF (default) would turn off the second approach. Only one of the two approaches should be active at any time.

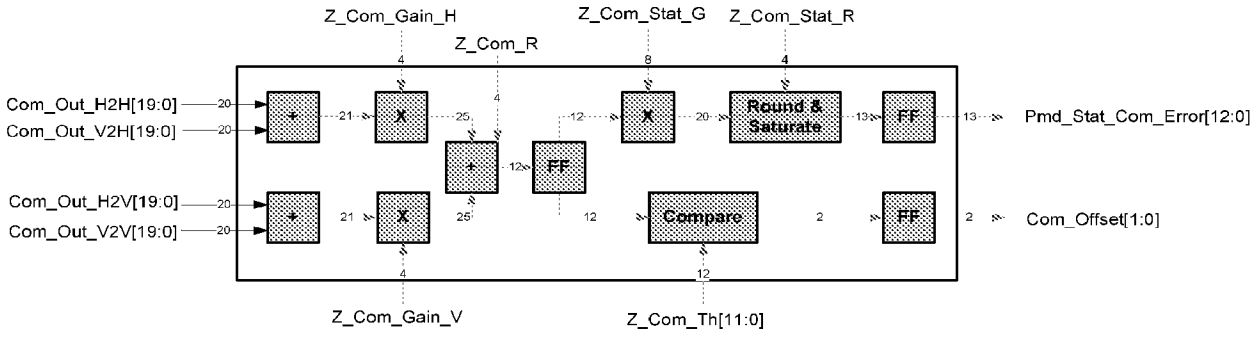


Figure 17. Operations performed for a PMD Tap update

The Tap Offset Control is responsible for regulating the shift of EQ filter taps in response to the CoM_Offset[1:0] or the polarization offset feedback coming from the FFS module. The polarization offset will have precedence over the CoM related offset. So if the polarization offset is being exercised the CoM offset should be ignored.

The design has a Tap_Offset Interface going from the **hlb_pmd_err** to the 8 **hlb_pmd_fir**. There is a unique 3-bit Tap_Offset_Indicator* for every **hlb_pmd_fir** for flexibility. The 3-bits are defined as:

- [0] : A data valid flag for offset. 0x0 (No offset required), 0x1(Offset)
- [1] : Direction of taps shift. 0x0 (New Tap [i] = Old Tap [i-2]), 0x1 (New Tap [i] = Old Tap [i+2])
- [2] : Active high blackout signal (generated by **hlb_pmd_err**) to block tap update during and right after transition

Based on the polarization or CoM offset the amount of shift to be performed will be conveyed to the **hlb_pmd_fir** using these Tap_Offset_Indicator* signals.

The CoM offset will only request shifts of one symbol (equivalent to 2 taps in the EQ filters) at a time which will require only one active high clock cycle of the data valid flag (Tap_Offset_Indicator*[0]) accompanied by the correct direction of the shift. Also the CoM offset will be the same for all the **hlb_pmd_fir.** The blackout signal (Tap_Offset_Indicator*[2]) should be kept high for 16 clock cycles to make sure the error updates generated using the older taps are flushed out of the design pipeline.

Also note that in case of Pol_Lock_Invalid being active only the V-pole needs to be reinitialized.

pmd_err_com_adjust

The **pmd_err_com_adjust** module is responsible for taking in the on-time samples (64 samples each for the 4 channels HI, HQ, VI and VQ) from the **pmd_err_out_accum**

module, making any adjustments (adding or deleting (if needed) a sample / symbol from the channels) based on the CoM offset and providing output on-time samples to the CFAT and CPR modules on a 64-sample per channel bus with either all samples valid or none on a clock cycle by clock cycle basis. A top-level block diagram of **pmd_err_com_adjust** is shown in Figure 18.

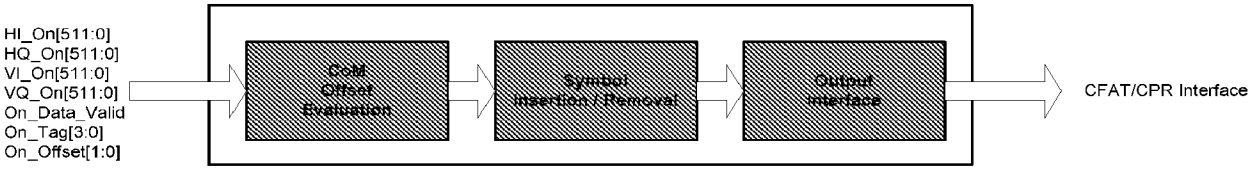


Figure 18. Operation stages inside pmd_err_com_adjust

The CoM Offset Evaluation looks at the On_Offset[1:0] signal and figures out that based on the CoM offset associated with the incoming data which of the following three actions need to be taken:

- Don't do anything (On_Offset[0] = 0 … there is no offset)
- Add a symbol (On_Offset = 2'd2)
- Remove a symbol (On_Offset = 2'd3)

Based on this decision the Symbol Insertion / Removal block will turn the incoming 64-samples per channel data bus into a 65-samples wide data bus where 63, 64 or 65 samples may be valid on any valid clock. This should just involve a simple 3-input mux for each sample. The addition / deletion of symbols will be same across the four channels (III, HQ, VI, VQ). Please note that the offset goes active for only once valid clock cycle per CoM offset event.

The Output Interface block needs to convert the 65-sample per channel wide data bus coming from the Symbol Insertion / Removal block to a 64-sample per channel wide data bus where either all or none of the samples are valid at any clock. This operation will involve a Barrel Shifter in some way / shape / form. Similar tasks are being tackled at various stages in the POLO design and so will refrain from discussing the implementation of this operation here. A common module written for project – wide use will be applied. As it turns out none of the other Barrel Shifters used elsewhere was applicable to this module so we tried to use as Designware shifter. That had issues during equivalency checking so we just created a Barrel Shifter with two multiplexor stages.

Please note that as the MFD module is performing a similar task at its output of going from a smaller number of data samples available per clock to a wider bus, it is guaranteed that we will have empty clock cycles (clock cycles where the Mfd_Data_Valid_* are 0) at least once every 32 clocks (or lesser) which will allow us to make sure that we do not overflow because of addition of extra symbols at this interface.

CoM Offset Evaluation and Symbol Insertion / Removal will be performed within a clock cycle. The Output Interface should take a minimum of 1 or maximum of 2 clock cycles.

Memory cut optimizations for decoder design

Problem Soft decision decoding designs require a lot of storage
For high speed implementation it translates into a large number of very wide but not too deep memories. Such memories are not very area efficient for ASIC implementation

Solution Modifications to TPC decoder design to repartition the distribution of data into memory to reduce the number of less efficient memory cuts.

Area and power savings for high-speed ASIC implementation

Technical Keywords Soft-decision decoder, TPC, Turbo codes

Novel This is a new technique. Can be used for any applications where TPC or other soft-decision decoders are used.

Inventors Lawrence Esker and Sameep Dave

The top-level of the SISO Full Iteration module instantiates two copies of the SISO axis-iteration as depicted in Figure 1. It also includes a bypass multiplexer and pipeline flops to help maintain timing closure. The top-level module will be provided in unencrypted form to allow full review by Ciena to tweak their system test and power reduction strategies.

The bypass logic enables a static selection of power reduction versus decoder BER performance system tradeoff. When bypass is enabled, the input ports will direct route to the output ports and a power-down control signal (for use as a gated clock enable via Synopsys Power Compiler) is generated.

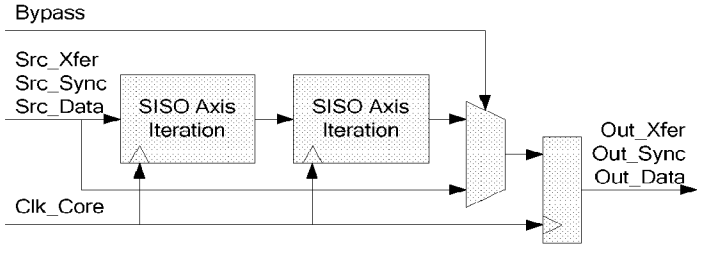


Figure 1. SISO Full Iteration with Bypass

A notional view of the SISO Axis Iteration is depicted in Figure 2.

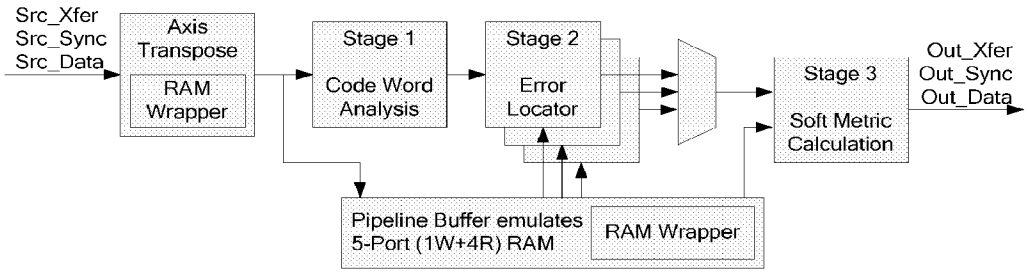


Figure 2. SISO Axis Iteration Notional View

The axis transpose RAM processes data at 256 elements per clock cycle. It simply swaps the rows and columns of the TPC such that consecutive iterations of the decoder can process the complete TPC block using replicated design for each axis iteration. The Axis Transpose contains two single port RAM arranged in a ping-pong, such that a block can be read in and another processed out simultaneously. The physical RAM implementation within the RAM Wrapper will break this up into multiple copies of narrower RAM as determined by the ASIC library.

Stages 1 and 3 of the decoder processes data at multiple elements per clock cycle. There are multiple parallel running copies of the decoder stages and pipeline buffer RAM assembly. Overall, the decoder processes a large number of elements per clock, required to meet the desired performance throughput at the target clock speed.

The decoder itself is highly pipelined such that while Stage 1 is analyzing a row of the TPC, stage 2 is examining the results of the previous row's analysis to locate errors. Stage 3 is computing soft metrics for an earlier row. As each row must be processed in a fixed number of clocks, there is not enough time for stage 2 to do its work. Multiple copies of stage 2 are staggered in time to enable extra clock cycles of error locating clocks.

To do their work, stage 2 and 3 require random access to the original input data that stage 1 had analyzed. As a result, a 5-port RAM must be emulated. This was accomplished in the design using five copies of single port RAM and multiplexers to route address and data to the appropriate RAM. Single port RAM is usually ideal for ASIC as it typically consumes the least area per bit.

While analyzing changes that would need to be made to the decoder for the high speed application, we discovered it is possible to alter the Pipeline Buffer topology from its original design.

- Current -- A single decoder's row pipeline buffer RAM is 5 copies of 14 words deep by 160 bits wide single port RAM.
- Alternate -- Stage 2 does not require access to all 160 bits. The 5-port emulation can be reduced to 80 bits wide. In addition, there is 1 copy of 80 words deep by 80 bits wide two-port RAM.

Due to the parallelism of the design, the per row RAM requirements are multiplied by 16 for a axis iteration and by 8 again for the complete design.

High speed SDFEC / TPC decoder design complexity is dictated by the memory as for highly parallel processing lots of soft-information needs the be written to / read out from memory on ever clock of data processing. Re-evaluating e memory cuts in the design to split up parts of information that need to be actively accesses versus parts that are rarely used and can be stowed away together helps drive the overall complexity as well as power consumption for the decoder design.

PMD Equalizer reseeding based on initial pole offset

Problem In optical fiber communications PMD (polarization mode dispersion) is a critical impairment.

Equalizer is required on the receiver side to track / correct PMD.

Big polarization offset during acquisition can cause the equalizer taps to converge such that when the PMD recovers to nominal values the taps are not centered leading to degraded performance.

Solution Algorithm for creating feedback from the framer / decoder to PMD equalizer to help shift the filter taps in accordance with the polarization offset during acquisition.

Ensures tap seeding such that during nominal PMD the equalizer can extract optimal performance

Technical Keywords PMD, Equalizer, Dual pole, PMQPSK, PM-DQPSK

Novel This is a new technique applicable to dual pole fiber communications.

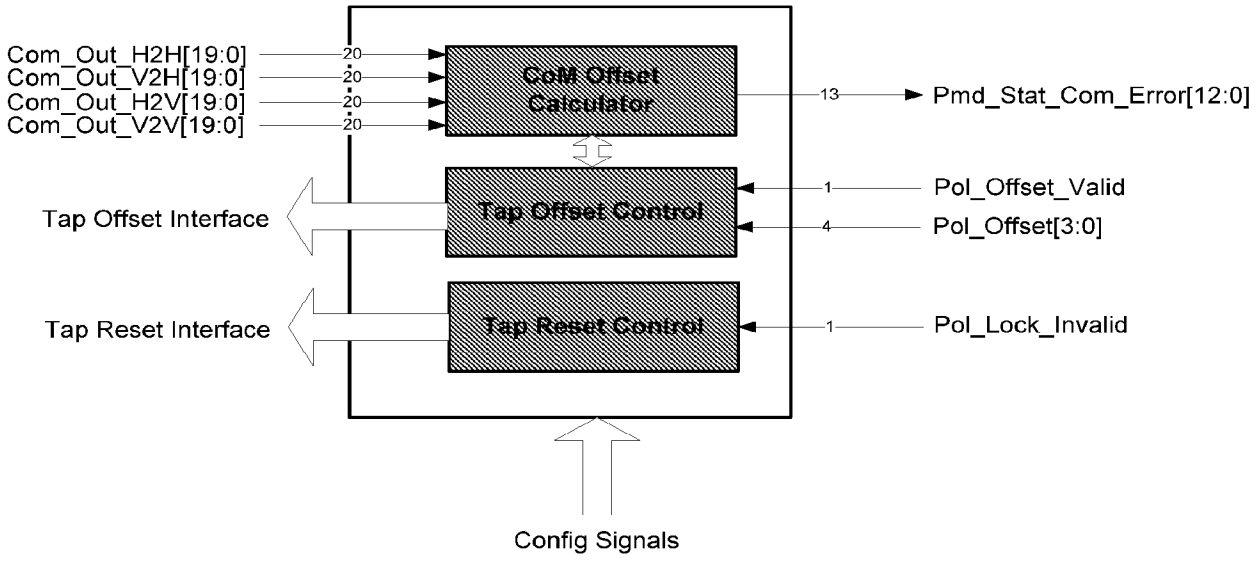
Inventors Fan Mo and Sameep Dave

PMD Equalizer reseeding based on initial pole offset

The PMD/PDL compensation / equalizer module utilizes adaptive equalization to compensate for the cross polarization interference, IQ channel interference, adjacent symbol interference introduced by PMD and PDL in optical channel and other residual impairments (like residual CD).

At initial acquisition stage if the UW detector / FFS detects a timing offset between the two poles it will convey that offset value to the EQ so that the filter taps can be re-initialized or shifted to compensate for the offset. This offset is performed in a balanced fashion between the filter taps generating the outputs for the two poles to make sure sufficient taps are available towards the edge of the filter.

If such compensation is not performed the EQ might converge such that during normal operation the higher weight taps (on one of the poles at any time) get skewed towards the edge of the filter essentially turning the EQ into a filter with small number of useful (relatively bigger value) taps.



The design has a Tap_Offset Interface going from the **hlb_pmd_err** to the 8 **hlb_pmd_fir**. There is a unique 3-bit Tap_Offset_Indicator* for every **hlb_pmd_fir** for flexibility. The 3-bits are defined as:

- [0] : A data valid flag for offset. 0x0 (No offset required), 0x1(Offset)
- [1] : Direction of taps shift. 0x0 (New Tap [i] = Old Tap [i-2]), 0x1 (New Tap [i] = Old Tap [i+2])
- [2] : Active high blackout signal (generated by **hlb_pmd_err**) to block tap update during and right after transition

The Polarization offset may request shifts of upto +/- 3 (could be any desired number) symbols at a time. And it will need different amounts of correction on the **hlb_pmd_fir** responsible for the H-pole (0, 2, 4, 6) output versus V-pole output (1, 3, 5, 7) as shown in **Error! Reference source not found.**. The number of active high clock cycle of the data valid flag (Tap_Offset_Indicator*[0]) required for a set of **hlb_pmd_fir** HLBs will be equal to the number of symbol shifts required for its taps. Because of taps needing to cross HLB boundaries during the shift the data valid should be sent as multiple 1 clock cycle wide pulses, once every 4 clock cycles. This will give enough time for the end taps from one HLB to transferred to the other HLB and be apart of the updated taps. The blackout signal (Tap_Offset_Indicator*[2]) should be kept high for 16 clock cycles to make sure the error updates generated using the older taps are flushed out of the design pipeline. Please note that Pol_Offset being positive means H pole is leading the V pol.

Table 1. Desired tap offsets based on Pol_Offset[3:0] / V-II offset from FFS

V - H offset	New Tap(i) for generating H	New Tap(i) for generating V
-6	Old Tap[i-6]	Old Tap[i+6]
-5	Old Tap[i-4]	Old Tap[i+6]
-4	Old Tap[i-4]	Old Tap[i+4]
-3	Old Tap[i-2]	Old Tap[i+4]
-2	Old Tap[i-2]	Old Tap[i+2]
-1	Old Tap[i]	Old Tap[i+2]
0	Old Tap[i]	Old Tap[i]
1	Old Tap[i+2]	Old Tap[i]
2	Old Tap[i+2]	Old Tap[i-2]
3	Old Tap[i+4]	Old Tap[i-2]
4	Old Tap[i+4]	Old Tap[i-4]
5	Old Tap[i+4]	Old Tap[i-4]
6	Old Tap[i+6]	Old Tap[i-6]

One trial per clock architecture for high speed TPC Decoding

Problem For very high speed TPC decoder designs high degree of parallelism is needed. The most complex processing stage in the TPC decoder is the processing stage where multiple trials / attempts at decoding are made. Decoding trials need to be spaced at t clocks where t is the correction capacity of the component BCH code. Requires duplicating the whole trial processing stage.

Solution Architecture change where selective replication of a small portion of the trial processing stage can allow to launch one trial per clock. Leads to significant reduction of overall decoder complexity.

Technical Keywords 100 G, TPC, Decoder, Chase

Novel This is a new architecture that can avoid needing multiple copies of the most complex section of the decoder design for high speed applications thus reducing complexity.

Inventors Sameep Dave and Lawrence Esker

One trial per clock architecture for high speed TPC Decoding

The top-level of the SISO Full Iteration module instantiates two copies of the SISO axis-iteration as depicted in Figure 1. It also includes a bypass multiplexer and pipeline flops to help maintain timing closure. The top-level module will be provided in unencrypted form to allow full review by Ciena to tweak their system test and power reduction strategies.

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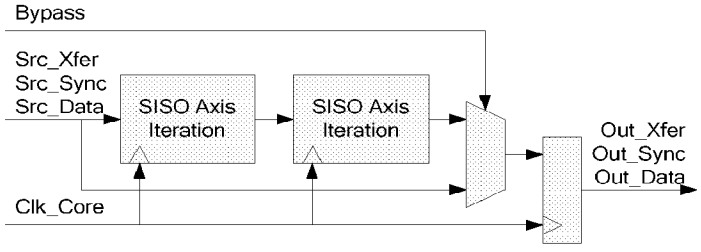

Figure 1. SISO Full Iteration with Bypass

A notional view of the SISO Axis Iteration is depicted in Figure 2.

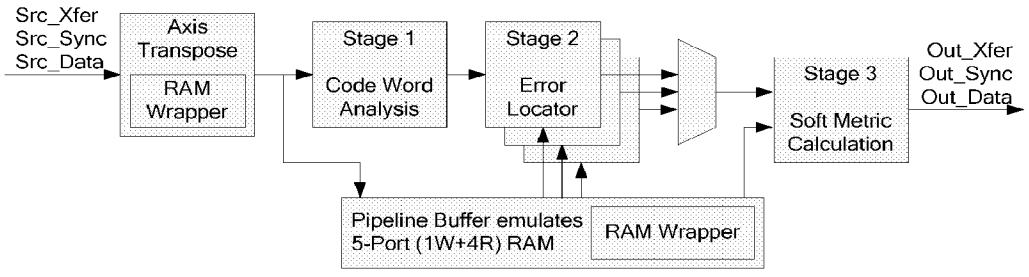

Figure 2. SISO Axis Iteration Notional View

The axis transpose RAM processes data at 256 elements per clock cycle. It simply swaps the rows and columns of the TPC such that consecutive iterations of the decoder can process the complete TPC block using replicated design for each axis iteration. The Axis Transpose contains two single port RAM arranged in a ping-pong, such that a block can be read in and another processed out simultaneously. The physical RAM implementation within the RAM Wrapper will break this up into multiple copies of narrower RAM as determined by the ASIC library.

Stages 1 and 3 of the decoder processes data at multiple elements per clock cycle. There are multiple parallel running copies of the decoder stages and pipeline buffer RAM assembly. Overall, the decoder processes a large number of elements per clock, required to meet the desired performance throughput at the target clock speed.

The decoder itself is highly pipelined such that while Stage 1 is analyzing a row of the TPC, stage 2 is examining the results of the previous row's analysis to locate errors. Stage 3 is computing soft metrics for an earlier row. As each row must be processed in a fixed number of clocks, there is not enough time for stage 2 to do its work. Multiple copies of stage 2 are staggered in time to enable extra clock cycles of error locating clocks.

Stage 2 is the most computationally intensive stage in the decoding process and needing multiple copies of this stage hugely impacts the overall decoder complexity. This invention proposes replication of just few pieces inside the stage 2 such that instead of every trial taking a few clock cycles, one trial can be launched per clock. This can drastically reduce the number of copies of the stage 2 of the decoding process for high speed applications leading to major savings in overall complexity.

One of the main reasons why trials take multiple clock cycles is that if a given trial finds a few error locations the logic has to access the soft information data from memory for these locations one by one to evaluate the effectiveness of the trial. Instead of doing this one-by-one for the various error locations if a multi-port memory is employed the information can be gathered within a clock cycle allowing the decoding to proceed at one trial per cycle.

Acronym/Abbreviation	Definition
ACT	Automatic Configuration Tool
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BPE	Block Phase Estimator
CD	Chromatic Dispersion
CDC	CD Compensation
CFAT	Carrier Frequency Acquisition and Tracking
CPR	Carrier Phase Recovery
DFT	Discrete Fourier Transform
DWDM	Dense Wavelength Division Multiplexing
ENOB	Effective Number Of Bits
EQ	Equalizer
FEC	Forward Error Correction
FFS	FEC Frame Synchronizer
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HDFEC	Hard Decision FEC
HI	I channel of Horizontal polarization
HQ	Q channel of Horizontal polarization
IFFT	Inverse FFT
IIR	Infinite Impulse Response
MFD	Matched Filter Decimator

NA	Not Applicable
NCO	Numerically Controlled Oscillator
PI	Proportional-Integral
PMD	Polarization Mode Dispersion
PP	Physical Partitions
QEF	Quadrature Error Filter
QPSK	Quadrature Phase Shift Keying
RLM	RTL Layout Macro
STAT	Symbol Timing Acquisition and Tracking
TBD	To Be Decided
TBR	To Be Reviewed
UW	Unique Word
UWH	Unique word inserted in the horizontal polarization
UWV	Unique word inserted in the vertical polarization
VI	I channel of Vertical polarization
VQ	Q channel of Vertical polarization

WHAT IS CLAIMED IS:

1. An apparatus and a method for high rate optical communication as described in the specification and figures.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	High Rate Optical Communication
First Named Inventor/Applicant Name:	Sameep Dave
Filer:	Charles Nicholas Pateros/Stacy Nguyen
Attorney Docket Number:	ECC-0452-US

Filed as Large Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional application filing	1005	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**220**

Electronic Acknowledgement Receipt

EFS ID:	9283569
Application Number:	61435278
International Application Number:	
Confirmation Number:	5581
Title of Invention:	High Rate Optical Communication
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	31864
Filer:	Charles Nicholas Pateros
Filer Authorized By:	
Attorney Docket Number:	ECC-0452-US
Receipt Date:	22-JAN-2011
Filing Date:	
Time Stamp:	11:19:23
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$220
RAM confirmation Number	8480
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

[Exhibit 1-66]

1	Provisional Cover Sheet (SB16)	FiledECC-0452ProvisionalSB.pdf	1060271 beb77e1e0613ca193fb87494bd6668a0567b0b69	no	4
Warnings:					
Information:					
2	Specification	FiledECC-0452-US-prov-app110121-1132a.pdf	523364 ffbc6a5b4ebffc9a6c3bba814519307d0d184575	no	55
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	28905 c9a12986eee7d6adb0ef7cc919ea5ba4863b1ed2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1612540		

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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Exhibit 2

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/521,263	08/08/2011		220	P001.12 (78120.0014)		

CONFIRMATION NO. 1904

16565
Holland & Hart LLP (ViaSat)
P.O. Box 8749
Denver, CO 80201

FILING RECEIPT

OC000000049400951

Date Mailed: 08/24/2011

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Fan Mo, Hinckley, OH;
Sameep Dave, Hinckley, OH;

Power of Attorney:
Michael Drapkin--55127

If Required, Foreign Filing License Granted: 08/18/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/521,263**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international

[Exhibit 2-69]

patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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Doc Code: TR.PROV
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

Inventor 1 Remove

Given Name	Middle Name	Family Name	City	State	Country i
Fan		Mo	Hinckley	OH	US

Inventor 2 Remove

Given Name	Middle Name	Family Name	City	State	Country i
Sameep		Dave	Hinckley	OH	US

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Title of Invention	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Attorney Docket Number (if applicable)	P001.12 (78120.0014)

Correspondence Address

Direct all correspondence to (select one):

◉ The address corresponding to Customer Number	○ Firm or Individual Name
Customer Number	16565

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

◉ No.

○ Yes, the name of the U.S. Government agency and the Government contract number are:

Doc Code: TR.PROV
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
Approved for use through 09/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

Entity Status

Applicant claims small entity status under 37 CFR 1.27

◯ Yes, applicant qualifies for small entity status under 37 CFR 1.27

◉ No

Warning

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Michael L. Drapkin/			Date (YYYY-MM-DD)	2011-08-08
First Name	Michael L.	Last Name	Drapkin	Registration Number (If appropriate)	55127

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P001.12 (78120.0014)
	Application Number	
Title of Invention	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Applicant 1 Remove

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Prefix	Given Name	Middle Name	Family Name	Suffix
	Fan		Mo	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Hinckley	State/Province	OH	Country of Residence[i]	US

Citizenship under 37 CFR 1.41(b)[i] CN

Mailing Address of Applicant:

Address 1	6155 El Camino Real		
Address 2			
City	Carlsbad	State/Province	CA
Postal Code	92009-1699	Country[i]	US

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sameep		Dave	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Hinckley	State/Province	OH	Country of Residence[i]	US

Citizenship under 37 CFR 1.41(b)[i] IN

Mailing Address of Applicant:

Address 1	6155 El Camino Real		
Address 2			
City	Carlsbad	State/Province	CA
Postal Code	92009-1699	Country[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P001.12 (78120.0014)
	Application Number	
Title of Invention	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS	

Customer Number	16565		
Email Address	patentdocket@hollandhart.com	Add Email	Remove Email

Application Information:

Title of the Invention	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS		
Attorney Docket Number	P001.12 (78120.0014)	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	9	**Suggested Figure for Publication (if any)**	

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☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

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Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P001.12 (78120.0014)
	Application Number	
Title of Invention	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS	

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Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
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Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	ViaSat, Inc.		
Mailing Address Information:			
Address 1	6155 El Camino Real		
Address 2			
City	Carlsbad	**State/Province**	CA
Country [i]	US	Postal Code	92009-1699
Phone Number		Fax Number	
Email Address			

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Signature:

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Signature	/Michael L. Drapkin/			Date (YYYY-MM-DD)	2011-08-08
First Name	Michael L.	Last Name	Drapkin	Registration Number	55127

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PATENT
ViaSat Docket No: ECC-0452-US-12
Attorney Docket No.: P001.12 (78120.0014)

FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS

BACKGROUND

[0001] The present disclosure relates to systems, devices, and methods for demodulation in fiber optic communications systems.

[0002] Fiber optic channels in network communications systems are widely deployed and are considered effective for data transmission, allowing relatively high bandwidth data communication. Optical fiber is typically flexible and can be bundled in cables. It is often used for long-distance communications because light propagates through the fiber with little attenuation compared to electrical cables. Typical present day commercial optical fiber systems transmit data at 10 or 40 Gbps. Each fiber can carry multiple independent channels, each using a different wavelength of light in a technique known as wavelength-division multiplexing (WDM).

[0003] Increased data transmission rates would be desirable as demand for bandwidth increases. However, in fiber optic systems, as data rates increase various optical phenomena begin to manifest and act to limit data transmission rates. For example, optical effects from chromatic dispersion (CD), polarization mode dispersion (PMD), and polarization dependent loss (PDL) begin to have a significant impact on the data transmission rate.

SUMMARY

[0004] Methods, systems, devices, and computer program products are described for formatting of data streams to be transmitted over fiber optic channels, and for processing received optical signals. An exemplary data transmission device may include a digital coding and modulation module that encodes a digital data stream, inserts unique words into the digital data stream, and modulates the encoded data stream and unique words onto a plurality of optical channels for transmission over an optical fiber. An exemplary demodulator and decoding device may include a unique word identification module that identifies the unique words inserted in each optical channel stream, determines one or more characteristics of the

plurality of optical channels based on the unique words, and provides the one or more characteristics to one or more other modules in the demodulator and decoding device. Other functionality may be implemented, as described in more detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] A further understanding of the nature and advantages of the present invention may be realized by reference to the following drawings. In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0006] FIG. 1 is a block diagram of an optical communication system including components configured according to various embodiments of the invention.

[0007] FIG. 2 is a block diagram of a digital coding and modulation unit according to various embodiments of the invention.

[0008] FIG. 3 is a block diagram of an alternate digital coding and modulation unit according to various embodiments of the invention.

[0009] FIG. 4 is a block diagram of exemplary incoming and outgoing streams from a unique word insertion module, differential encoding module, and associated transmission optical interface module according to various embodiments of the invention.

[0010] FIG. 5 is a illustration of a bit stream used to insert unique words into dual-polarity QPSK channels block diagram of a digital coding and modulation unit according to various embodiments of the invention.

[0011] FIG. 6 is a block diagram of a digital demodulation and decoding unit according to various embodiments of the invention.

[0012] FIG. 7 is a block diagram of a digital demodulation unit according to various embodiments of the invention.

[0013] FIG. 8 is a flow chart of a method for inserting a unique word into optical streams to be transmitted over optical fibers according to various embodiments of the invention.

[0014] FIG. 9 is a flow chart of a method for digital demodulation of optical signals based on signal characteristics determined from identification of unique words present on a plurality of optical channels according to various embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Methods, systems, devices, and computer program products are described for formatting of data streams to be transmitted over fiber optic channels, and for processing received optical signals. An exemplary data transmission device may include a digital coding and modulation module that encodes a digital data stream, inserts unique words into the digital data stream, and modulates the encoded data stream and unique words onto a plurality of optical channels for transmission over an optical fiber. An exemplary demodulator and decoding device may include a unique word identification module that identifies the unique words inserted in each optical channel stream, determines one or more characteristics of the plurality of optical channels based on the unique words, and provides the one or more characteristics to one or more other modules in the demodulator and decoding device. Additional functionality may be implemented, as described in more detail below.

[0016] This description provides examples, and is not intended to limit the scope, applicability or configuration of the invention. Rather, the ensuing description will provide those skilled in the art with an enabling description for implementing embodiments of the invention. Various changes may be made in the function and arrangement of elements.

[0017] Thus, various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that the methods may be performed in an order different than that described, and that various steps may be added, omitted or combined. Also, aspects and elements described with respect to certain embodiments may be combined in various other embodiments. It should also be appreciated that the following systems, methods, devices, and software may individually or collectively be components of a larger system, wherein other procedures may take precedence over or otherwise modify their application.

[0018] Systems, devices, methods, and software are described for an optical communication system that utilizes fiber optic optical cables as a data transmission medium. An example of an optical data transport system 100 is illustrated in **FIG. 1**. In this embodiment, the optical data transport system 100 includes a data source that provides data

to a digital coding and modulation unit 105. The data source may include any of a number of common data sources, such as a user telecommunications device, a cable operator head-end unit, a telecommunications provider central office, a computer server, or a network attached storage system, to name but a few examples. In many embodiments, the data source generates significant quantities of data to be transported across the optical data transport system 100. The digital coding and modulation unit 105 receives this data, and performs framing, forward error correction coding, and modulation functions on the data. In various embodiments, the digital coding and modulation unit 105 inserts a unique word into the data stream for each optical channel over which data will be sent. The electrical-to-optical (E-O) unit 110 transforms the data and inserted unique words into optical signals, and transmits optical signals containing the data via a fiber connection 115. The fiber connection 115 may include well known components of such connections, including a fiber optic cable. An optical-to-electrical (O-E) unit 120 receives the optical signal from the fiber connection 115, and transforms the data into the electrical domain. The digital demodulation and decoding unit 120 receives the digitized version of the optical signal and detects the unique words that are inserted onto each optical channel. The detection of the unique words on each channel can be used to provide characteristics of the optical channels that may be used to the digital demodulation and decoding unit 120 when performing demodulation, forward error correction decoding, and de-framing functions on the data from the optical signal. The digital demodulation and decoding unit 120 may then output the data (e.g., to a user telecommunications device, a cable operator head-end unit, a telecommunications provider central office, a computer server, or a network attached storage system).

[0019] **FIG. 2** illustrates a digital coding and modulation unit 105-a. In the illustrated embodiment, the digital coding and modulation unit 105-a includes a data transport layer framer module 205, a FIFO module 210, an FEC coder module 215, an interleaving module 220, a unique word insertion module 225, a differential encoding module 230, and a transmitter optical interface module 235. The data transport layer framer module 205 may place the data received from the data source into packet frames for transmission. The packet frames may conform to one of many common protocols for packet frames used in optical communications systems which commonly include a header and a payload, and possibly a trailer, such as a CRC. As is well understood, the header may be interleaved with the payload during transmission, depending upon the particular protocol being used for optical transmission. The FIFO module 210 queues the packet frames received from the data

transport layer framer module 205. The FEC coder module 215 calculates and adds forward error correction (FEC) information to the frames of data received from the data transport layer framer module 205. The particular type of FEC information of various embodiments generally includes systematically generated redundant error-correcting code (ECC) data that is transmitted along with the frames, and in an embodiment FEC information includes turbo product code (TPC) information. Interleaving module 220, in the embodiment of Fig. 2, receives the FEC information and frames of data, and interleaves the FEC information with the frames of data to reduce the likelihood of a channel error removing all FEC data for a particular frame. Unique word insertion module 225, in the embodiment of Fig. 2, inserts unique words into the data stream received from the interleaving module 220. Unique words may be added to each transmitted optical channel to assist with the decoding and demodulation of the optical signals containing different streams of data. In one embodiment, the interleaved frames of data are modulated using dual-polarity (dual-pole) quadrature-phase-shift-keying (QPSK), resulting in four optical channels. The unique word insertion module 225 of this embodiment inserts a unique word into the data stream for each of the four optical channels. The inserted unique word is a different unique word for each optical channel, that is inserted into the data stream for the optical channel periodically. Differential encoding module 230 provides differential encoding for the interleaved FEC encoded frames and unique words. Differential encoding is a well known technique in which data to be transmitted depend not only on the current bit (or symbol), but also on the previous one, such as through an exclusive OR function. The differentially encoded data is then provided to the transmitter optical interface module 235. The transmitter optical interface module 235 may forward the modulated data to the E-O module (Fig. 1) where it may be transmitted in the optical domain via dual-pole QPSK modulation, resulting in four parallel optical streams. Other modulation schemes may be used in other examples, as well.

[0020] As will be readily understood by one of skill in the art, the particular arrangement of the modules of FIG. 2 are exemplary, and the particular order in which data is processed may vary, and particular functions of various modules may be modified and/or combined. An exemplary alternative configuration of a digital coding and modulation unit 105-b is illustrated in **FIG. 3**. In this exemplary embodiment, the digital coding and modulation unit 105-b includes the modules as described with respect to digital coding and modulation unit 105-a of FIG. 2, arranged in an alternate order. In the example of FIG. 3, the digital coding and modulation unit 105-b includes a data transport layer framer module 305, a FIFO module

310, an FEC coder module 315, an interleaving module 320, a differential encoding module 325, a unique word insertion module 330, and a transmitter optical interface module 335. In this particular example, differential encoding module 325 receives data from interleaving module 320. Differential encoding module 325 provides differential encoding for the interleaved FEC encoded frames, which is then provided to unique word insertion module 330. Unique word insertion module 330, in the embodiment of FIG. 3, inserts unique words into the differentially encoded data stream received from the differential encoding module 325. Similarly as discussed with respect to FIG. 2, unique words may be added to each transmitted optical channel to assist with the decoding and demodulation of the optical signals containing different streams of data. In one embodiment, the interleaved frames of data are modulated using dual-pole QPSK, resulting in four optical channels, and the unique word insertion module 330 inserts a unique word into the data stream for each of the four optical channels, and provide the data stream to the transmitter optical interface module 335. In the embodiment of FIG. 3, the transmitter optical interface module 335 modulates the data onto a number of optical channels and forwards the modulated data to the E-O module (Fig. 1) where it may be transmitted in the optical domain via dual-pole QPSK modulation, resulting in four parallel optical streams. Other modulation schemes may be used in other examples, as well.

[0021] The unique word insertion module 225 of FIG. 2, as briefly discussed, inserts a unique word into each data stream corresponding to each transmitted optical channel. It is noted that unique word insertion module 330 of FIG. 3 operates in a similar manner, and various aspects of the unique word insertion module 225 will be described in more detail with the understanding that such discussion applies equally to unique word insertion module 330. With reference now to **FIG. 4**, an illustration of incoming and outgoing data streams 400 of unique word insertion module 225-a, differential encoding module 230-a, and transmitter optical interface module 235-a, is described. In this example, an interleaved FEC encoded bit (or symbol) stream 405 is received at unique word insertion module 225-a. Similarly as described above, unique word insertion module 225-a inserts unique words into the stream 405, and provides the stream and unique words to differential encoding module 230-a, which provides a differentially encoded stream to transmitter optical interface module 235-a. The transmitter optical interface module 235-a may modulate the incoming data stream onto different optical channels according to various modulation techniques. In one example, the incoming data stream is modulated using dual-pole QPSK onto four different optical

channels, namely a horizontal in-phase (HI) channel, a horizontal quadrature (HQ) channel, vertical in-phase (VI) channel, and a vertical quadrature (VQ) channel. Data transmitted on each of the optical channels may be selected, for example, by taking a first received bit (or symbol) and modulating it onto the HI channel, taking the second received bit and modulating it onto the HQ channel, and so on. In such an embodiment, the unique word insertion module 225-a inserts unique word bits into the data stream periodically to produce output data streams for each channel that have periodic unique words embedded therein. The output from the transmitter optical interface module 235-a thus provides an HI data stream 410 that has a first unique word periodically included therein, an HQ data stream 415 that has a second unique word periodically included therein, a VI data stream 420 that has a third unique word periodically included therein, and a VQ data stream 425 that has a fourth unique word periodically included therein. Each of the first, second, third, and fourth unique words are selected to uniquely identify the particular data stream associated with the unique word. When the transmitted optical signals are received at a receiver, these unique words may be identified and assist with compensation and demodulation of received optical signals. In one embodiment, the unique words include pseudonoise (PN) code generated for the unique word in each data stream 410 through 425.

[0022] The unique word insertion module 225-a inserts bits of data into the incoming interleaved FEC encoded bit stream 405 such that data streams 410 through 425 each include the correct corresponding unique word. As mentioned, the transmitter optical interface module 235-a may modulate consecutively received bits onto separate HI, HQ, VI, and VQ data streams. In such a case, the unique word insertion module 225-a inserts a bit stream into the interleaved FEC encoded bit stream 405 in which each fourth bit corresponds to a particular unique word. An example of such a unique word insertion bit stream 500 is illustrated in **FIG. 5**. In this example, each unique word is n/4 bits in length, resulting in unique word insertion bit stream 500 that is n bits. These n bits are periodically inserted into the incoming interleaved FEC encoded bit stream 405 according to a predetermined interval, with bits 1, 5, 9, and so on through bit n-3 corresponding to the first unique word (UW1) of HI data stream 410. Likewise, bits 2, 6, 10, and so on through bit n-2 correspond to the second unique word (UW2) of HQ data stream 415; bits 3, 7, 11, and so on through bit n-1 correspond to the third unique word (UW3) of VI data stream 420; and bits 4, 8, 12, and so on through bit n correspond to the fourth unique word (UW4) of VQ data stream 425. Of course, other modulation techniques may be used in which data is modulated onto optical

channels according to different sequences, and the unique word insertion module 225-a provides the unique word insertion bit stream accordingly so as to provide each optical channel with a corresponding unique word.

[0023] As illustrated in **FIG. 6**, a digital demodulation and decoding unit 125-a may include a number of modules. In this embodiment the digital demodulation and decoding unit 125-a includes a receiver optical interface module 605, a unique word identification module 610, demodulator module 615, an FEC decoder module 620, and a data transport layer de-framer module 625. The receiver optical interface 605 is the interface from the O-E unit 120. The receiver optical interface module 605 provides electrical signals to a unique word identification module 610 that identifies the unique words that are inserted in each of the optical channel data streams. The unique word identification module 610 removes the unique words from each respective data stream, and determines information related to the received data streams that may be derived from the unique word identification, such as the particular received channel on which the unique words are identified, and the timing of the receipt of the unique words. This information may be provided to other modules for assistance in the demodulating and/or decoding of the received optical channels. The electrical signals, are provided from the unique word identification module 610 to demodulator module 615. Demodulator module 615 may include a differential decoding module that decodes differential encoding that may have been performed at digital coding and modulation module 105. Various embodiments of the demodulator module 615 will be discussed in further detail below. The information from the demodulator module 615 is provided to FEC decoder module 620 which decodes and may correct transmission errors identified from error-correcting code. The FEC decoder module 620 provides decoded data to the data transport layer de-framer module 625, which de-frames the data from the signal according to the particular protocol used in the optical transmission, and provides output data. The data output may be, for example, a user or any receiving system.

[0024] These components of may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs) and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be

implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0025] Referring now to **FIG. 7**, a demodulator unit 700 is described. This may be the digital demodulator unit 615 of FIG. 6. In this example, two polarization components are received, one horizontal component (H) and one vertical component (V). Each of the H and V components includes both an in-phase (I) component and a quadrature (Q) component. For reference, the two components in the horizontal polarization are referred to as HI (horizontal in-phase component) and HQ (horizontal quadrature component). Similarly, the two components in the vertical polarization are referred to as VI (vertical in-phase component) and VQ (vertical quadrature component). The demodulator unit 800 processes the digitized samples of the I and Q components of the two polarization components to recover the transmitted data. At the input, the demodulator unit 700 accepts the four parallel streams carrying HI, HQ, VI and VQ samples. In one embodiment, each stream contains multiple samples per clock. At its output the demodulator may provide demodulated hard-decision data (although in other examples, soft-decision data may be provided) to the FEC decoder module. The demodulator unit 700 may identify the beginning of a FEC frame. Additionally, in some embodiments the demodulator unit 700 receives feedback signals from the FEC decoder module 620 regarding the convergence status for error correction. Furthermore, in some embodiments the demodulator unit 700 receives information from unique word identification module 610 to assist in the demodulation.

[0026] In some embodiments, the demodulator unit 700 is implemented as an application specific integrated circuit (ASIC) that includes a number of functional modules. In such embodiments, the demodulator unit 700 may have a control and monitor interface bus 705 connected to a host processor 710 allowing for configuration of demodulator parameters (filter coefficients, loop gains, etc.) and extraction of demodulator status. With continuing reference to FIG. 7, several of the sub-modules within the demodulator unit 700 of various embodiments are described. In this embodiment, a quadrature error filter (QEF) module 715 provides a collection of data formatting, error detection and correction functions. In one embodiment, input data samples are expected to be in binary-offset /offset-binary format and are converted to a two's complement (2C) format for processing within a digital signal processor. The incoming HI, HQ, VI and VQ streams, in some embodiments, also can be independently swapped and inverted if needed, allowing for any design issues that might translate into an accidental inversion or IQ swap. Each data stream of these various

embodiments may be processed to remove polarization skew (between H and V poles) as well as I-Q skew within a pole. The QEF module 715 may provide for detection and removal of four types of quadrature signal errors: I/Q Skew, DC bias, I/Q amplitude imbalance, and I/Q phase imbalance. All four error detectors may be independently enabled or disabled, in some embodiments, via the processor interface, and the detected error values are output as status values via this same interface. The QEF module 715 may also output a gain control signal that may be used by other components of the system.

[0027] The QEF module 715 is connected with a frequency offset removal module 720. The frequency offset removal module 720 in one example performs a frequency rotation on the data samples coming out of the QEF module 715. The amount of frequency rotation is controlled by a frequency error input that is sourced by a carrier frequency acquisition and tracking (CFAT) module 740. Such frequency offset removal function may remove residual frequency left from the LO laser tuning in the optical domain. A chromatic dispersion compensation module 725 removes bulk chromatic dispersion from the horizontal and vertical polarization channels. The compensation may be applied via a filter in the frequency domain. The amount of correction may be controlled by the chromatic dispersion filter inputs that are derived outside of the demodulator module 700 and provided via the host processor 710 and control and monitor interface bus 705, in this embodiment.

[0028] A matched filter decimator (MFD) module 730 may implement an interpolation function that provides decimation on samples taken at two+ε times the symbol rate. In one embodiment, each of the four data streams has an independent bank of FIR filters with selected coefficients. The incoming data is processed through the filter banks to produce two samples per symbol for each data stream. Data samples are gathered and assembled into blocks of fixed numbers of samples per stream per clock by a sample block assembler. The assembly function may be identical for the I and Q streams in each polarization so one assembly block may service two streams. A PMD/PDL compensation module 735 may utilize adaptive equalization to compensate for cross-polarization interference, IQ channel interference, and adjacent symbol interference introduced by PMD and PDL in the optical channel and other residual impairments, such as residual chromatic dispersion as mentioned above. In one embodiment, an adaptive equalizer takes in data at one or two samples/symbols from the MFD module 730 and processes the data through a bank of FIR filters with adaptive filter tap coefficients.

[0029] In some embodiments, a symbol timing acquisition and tracking (STAT) module 745 may estimate symbol timing using an early/late symbol radius matching scheme and PI controller, and generate an error signal to correct symbol timing. This STAT module 745, in an embodiment, also has a symbol timing lock detection mechanism that outputs a symbol lock indicator. In various embodiments, there are two sets of gains for the PI controller (wide band for acquisition and narrow band for tracking). When not in timing lock, the wideband gains may be used, otherwise, the narrowband gains may be used. The STAT module 745 may perform symbol timing acquisition and tracking of a portion of the optical signal after the PMD/ PDL compensation module compensates for interference caused by PMD and PDL and before carrier phase recovery on the portion of the optical signal.

[0030] The CFAT module 740 may be responsible for acquiring, as well as tracking, carrier frequency. Carrier frequency acquisition is achieved using one of a number of techniques, such as through fast Fourier transform (FFT) with appropriate averaging and peak frequency component detection. The CFAT module 740 may provide a frequency error input to the frequency offset removal module 720. The CFAT module 740, in some embodiments, also provides a control output for the local oscillator (LO) frequency offset output, that may be used with data from the frame synchronization and interface module 760. A carrier phase tracking and recovery module 750 may use a feed-forward algorithm with a block phase estimator and a phase rotation function to remove residual frequency and phase errors. The carrier phase tracking and recovery module 750 may operate on the on-time data samples produced by the PMD compensation module. A differential decoder 755 may be responsible, in various embodiments, for accepting symbol streams from the carrier phase tracking and recovery module 750 (e.g., at 1 sample per symbol). The differential decoder 755 may be configured to differentially decode the signal and provide the decoded output (e.g., a hard-decision output data stream) to the frame synchronization and interface module 760. The frame synchronization and interface module 760 processes data to achieve frame synchronization, and may include functional blocks for data alignment, frame sync detection, and clock transfer. The frame synchronization module 760 may be configured to skew, swap, and rotate received channels with respect to each other. In some embodiments the frame synchronization module 760 receives information from unique word identification module 610 to assist in data alignment, frame sync detection, and/or clock transfer.

[0031] **FIG. 8** is a flow chart of a method 800 for digital modulation and encoding of an optical signal according to various embodiments of the invention. The method 800 may be performed by the digital modulation and encoding unit 105 of FIGs. 1 through 3.

[0032] At block 805, incoming data is received. Incoming data may be generated from a data source that provides data to a digital coding and modulation unit, such as unit 105 of FIG. 1. The data source may include any of a number of common data sources, such as a user telecommunications device, a cable operator head-end unit, a telecommunications provider central office, a computer server, or a network attached storage system, to name but a few examples. At block 810, the received data is formatted into packet frames for transmission. The packet frames may conform to one of many common protocols for packet frames used in optical communications systems which commonly include a header and a payload, and possibly a trailer, such as a CRC. As is well understood, the header may be interleaved with the payload during transmission, depending upon the particular protocol being used for optical transmission. At block 815, the stream of packet frames is encoded with forward error correction code (FEC) to generate an encoded but stream. The particular type of FEC information of various embodiments generally includes systematically generated redundant error-correcting code (ECC) data that is transmitted along with the frames, and in an embodiment FEC information includes turbo product code (TPC) information. The FEC information may be interleaved with the frames of data to reduce the likelihood of a channel error removing all FEC data for a particular frame. At block 820, a unique word is inserted into the encoded bit stream for each transmitted optical channel. Such unique words may assist with the decoding and demodulation of the optical signals containing different streams of data. In one embodiment, the interleaved frames of data are modulated using dual-polarity (dual-pole) quadrature-phase-shift-keying (QPSK), resulting in four optical channels, with a unique word inserted into the data stream for each of the four optical channels. Differential encoding may be applied to the bit stream either before or after the addition of the unique words. The encoded data streams and unique words transmitted over an optical fiber connection, as indicated at block 825. Transmission may be performed in the optical domain via dual-pole QPSK modulation, resulting in four parallel optical streams. Other modulation schemes may be used in other examples, as well.

[0033] **FIG. 9** is a flow chart of a method for digital demodulation of an optical signal according to various embodiments of the invention. The method 900 may be performed by

the digital demodulation and decoding unit 125 of FIG. 1 or 6. More specifically, the method 900 may be performed by the demodulator unit 615, or 700 of FIG. 6 or 7, respectively.

[0034] At block 905, a digitized version of an optical signal is received, including four parallel streams: a horizontal in-phase (HI) stream, a vertical in-phase stream (VI), a horizontal quadrature (HQ) stream, and a vertical quadrature (VQ) stream. At block 910, a unique word in each of the four parallel streams is identified. At block 915, characteristics of the parallel data streams are determined based on the identification of the unique words. Such characteristics may include, for example, the particular received channel on which the unique words are identified, and the timing of the receipt of the unique words. At block 920, the data streams are demodulated into data transport frames using, in part, characteristics of the optical signals determined using the identified unique words. In various embodiments, one or more modules within an demodulator and decoder may receive one or more measured characteristics of the parallel data streams that were determined based on the identification of the unique words, which may be used to assist in the demodulating and/or decoding of the received optical channels.

[0035] These components may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs) and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0036] It should be noted that the methods, systems and devices discussed above are intended merely to be examples. It must be stressed that various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that, in alternative embodiments, the methods may be performed in an order different from that described, and that various steps may be added, omitted or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner. Also, it should be emphasized that technology evolves and, thus, many of

the elements are exemplary in nature and should not be interpreted to limit the scope of the invention.

[0037] Specific details are given in the description to provide a thorough understanding of the embodiments. However, it will be understood by one of ordinary skill in the art that the embodiments may be practiced without these specific details. For example, well-known circuits, processes, algorithms, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments.

[0038] Also, it is noted that the embodiments may be described as a process which is depicted as a flow diagram or block diagram. Although each may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may have additional steps not included in the figure.

[0039] Moreover, as disclosed herein, the term "memory" may represent one or more devices for storing data, including read-only memory (ROM), random access memory (RAM), magnetic RAM, core memory, magnetic disk storage mediums, optical storage mediums, flash memory devices or other computer-readable mediums for storing information. The term "computer-readable medium" includes, but is not limited to, portable or fixed storage devices, optical storage devices, wireless channels, a sim card, other smart cards, and various other mediums capable of storing, containing or carrying instructions or data.

[0040] Furthermore, embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When implemented in software, firmware, middleware or microcode, the program code or code segments to perform the necessary tasks may be stored in a computer-readable medium such as a storage medium. Processors may perform the necessary tasks.

[0041] Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. For example, the above elements may merely be a component of a larger system, wherein other rules may take precedence over or otherwise modify the application of the invention. Also, a number of steps may be undertaken before, during, or after the above elements are considered. Accordingly, the above description should not be taken as limiting the scope of the invention.

WHAT IS CLAIMED IS:

1. A system, apparatus, or method as described in the Specification and/or Drawings.

[Exhibit 2-93]

ABSTRACT OF THE DISCLOSURE

Methods, systems, and devices are described for formatting of data streams to be transmitted over fiber optic channels, and for processing received optical signals. An exemplary data transmission device may include a digital coding and modulation module that encodes a digital data stream, inserts unique words into the digital data stream, and modulates the encoded data stream and unique words onto a plurality of optical channels for transmission over an optical fiber. An exemplary demodulator and decoding device may include a unique word identification module that identifies the unique words inserted in each optical channel stream, determines one or more characteristics of the plurality of optical channels based on the unique words, and provides the one or more characteristics to one or more other modules in the demodulator and decoding device.

5198130_1.DOC

Title: FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Inventor: Dave et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 1 of 9

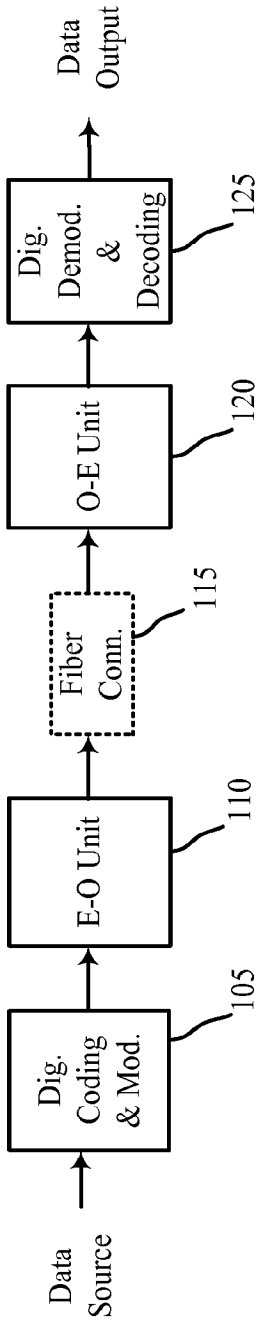

FIG. 1

Title: FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Inventor: Dave et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 2 of 9

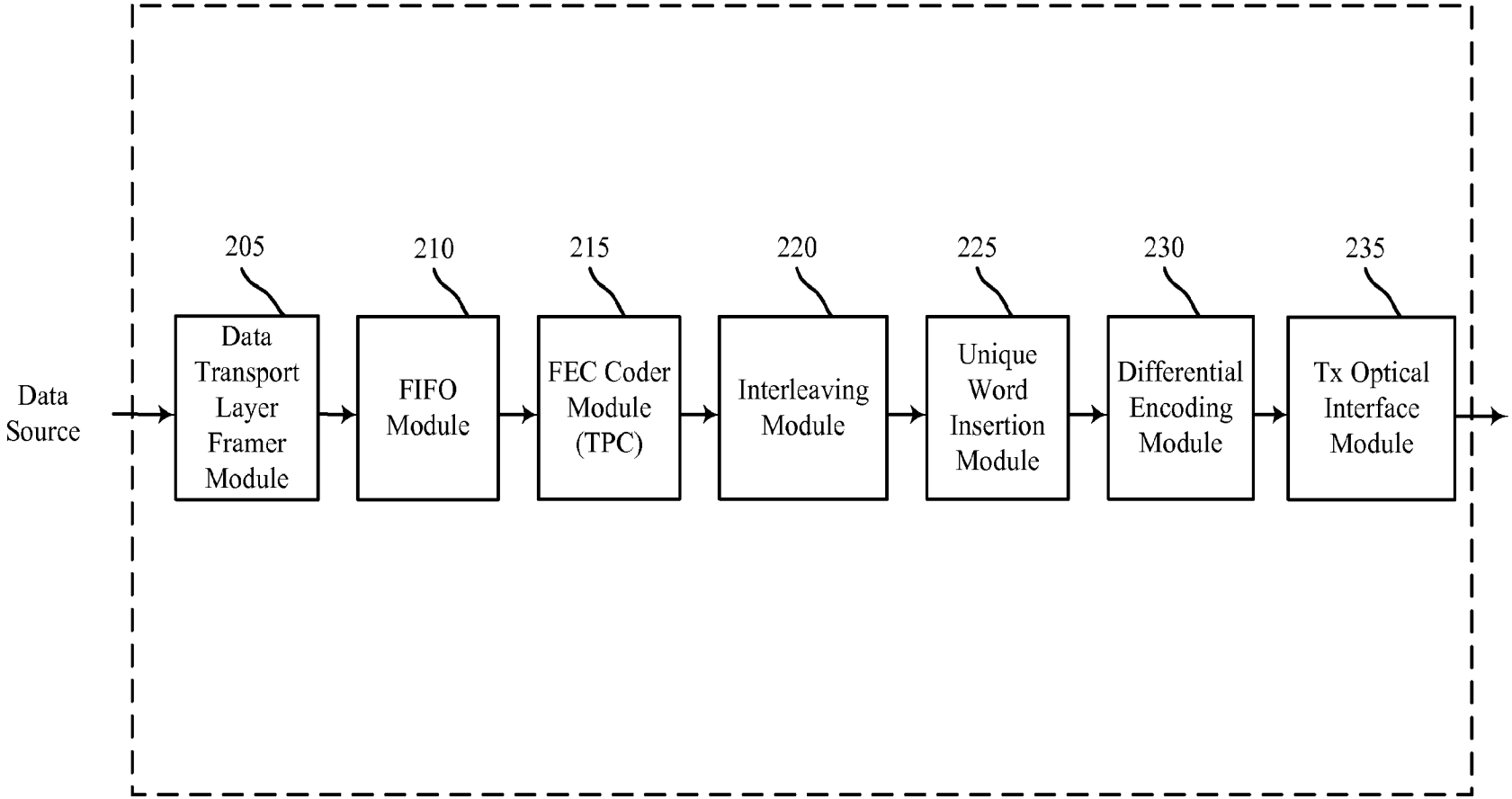

FIG. 2

105-a

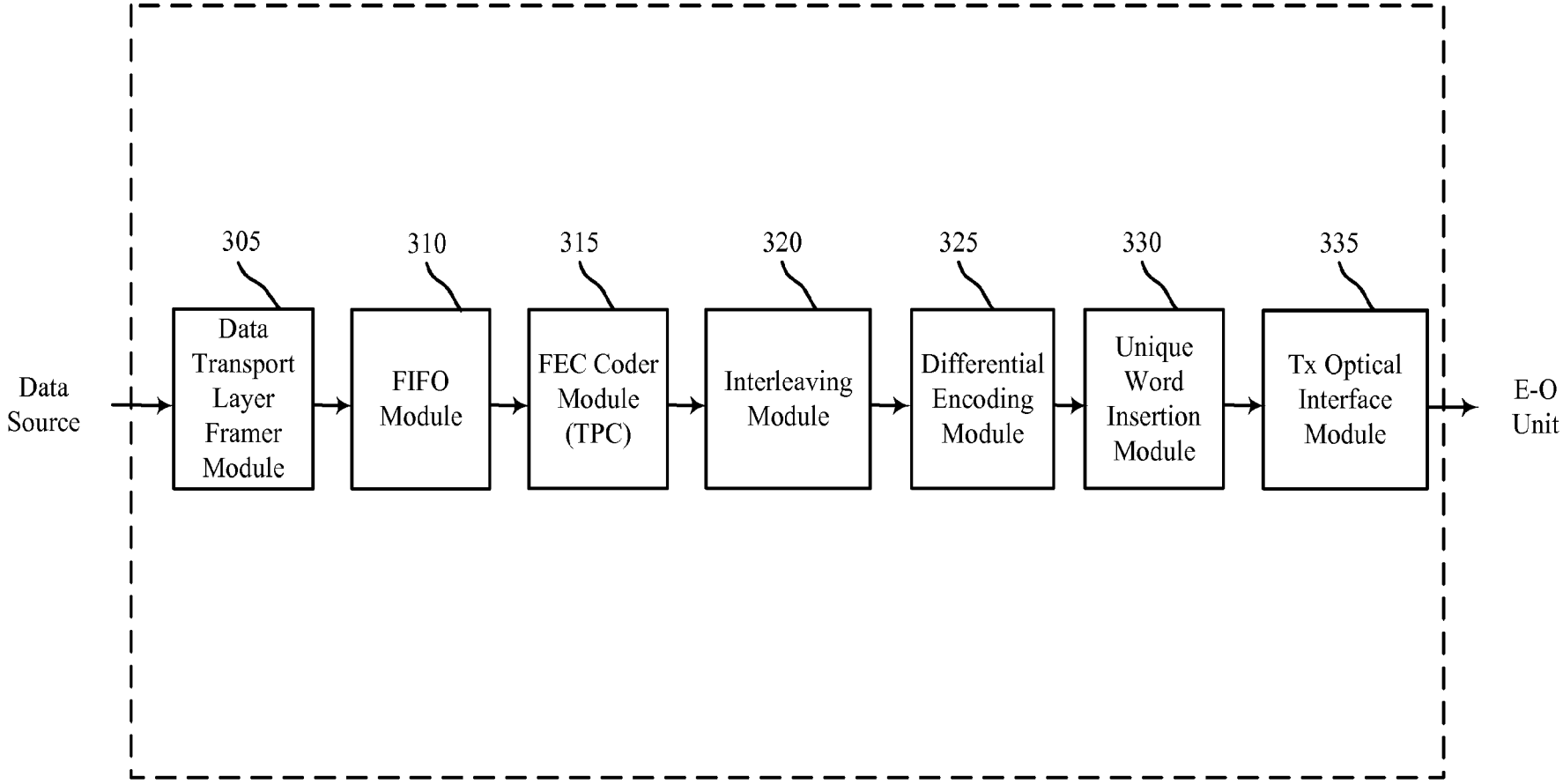

FIG. 3

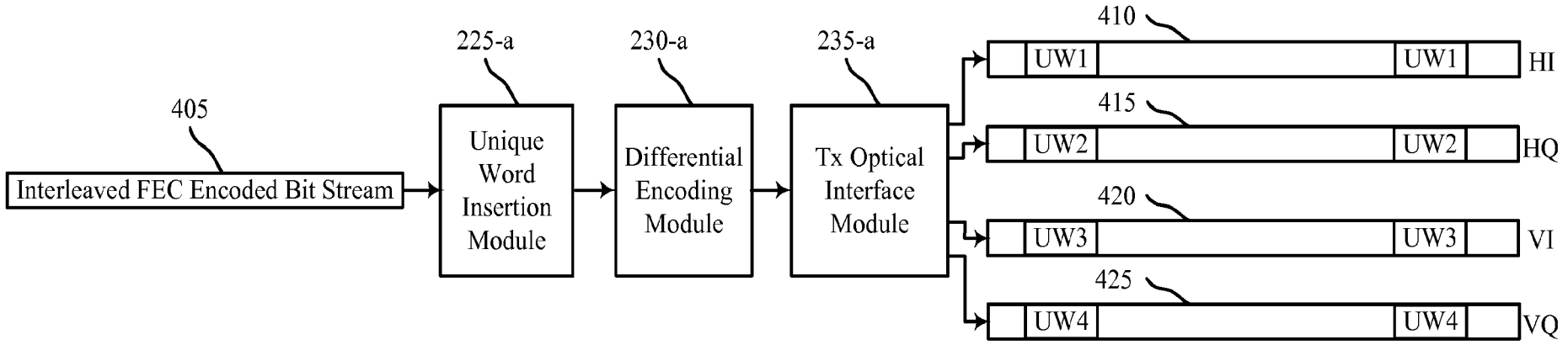

FIG. 4

400

Title: FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Inventor: Dave et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 4 of 9

Title: FRAME FORMATTING FOR HIGH-RATE OPTICAL COMMUNICATIONS
Inventor: Shive et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 5 of 9

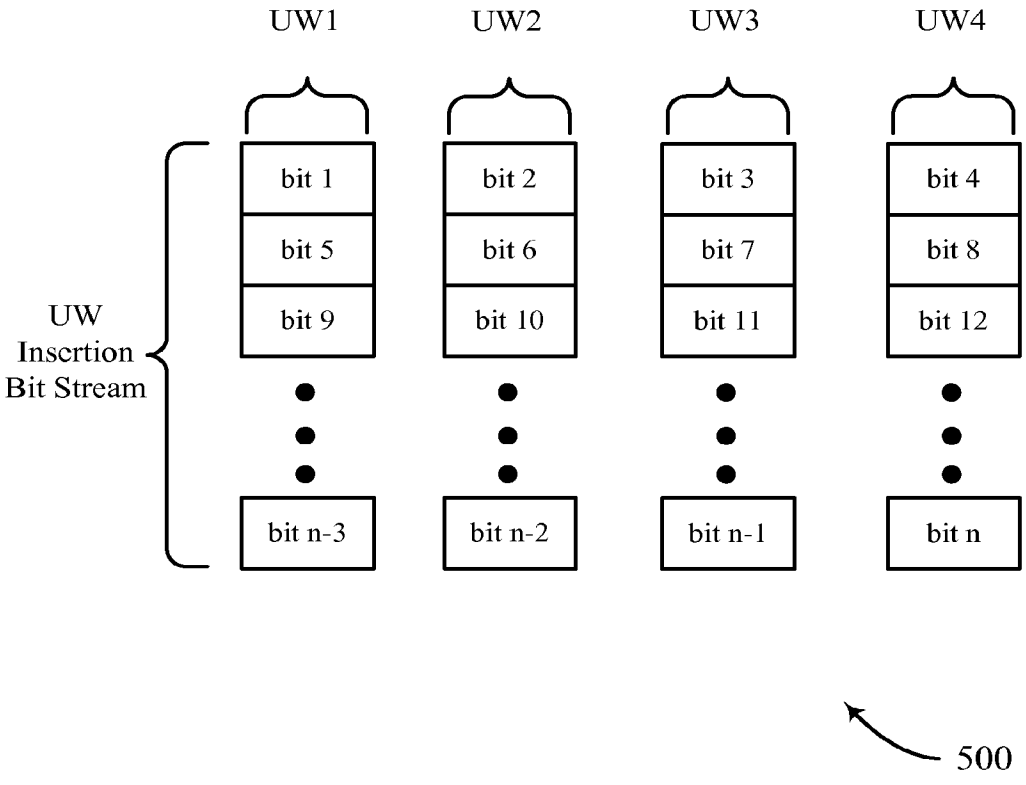

FIG. 5

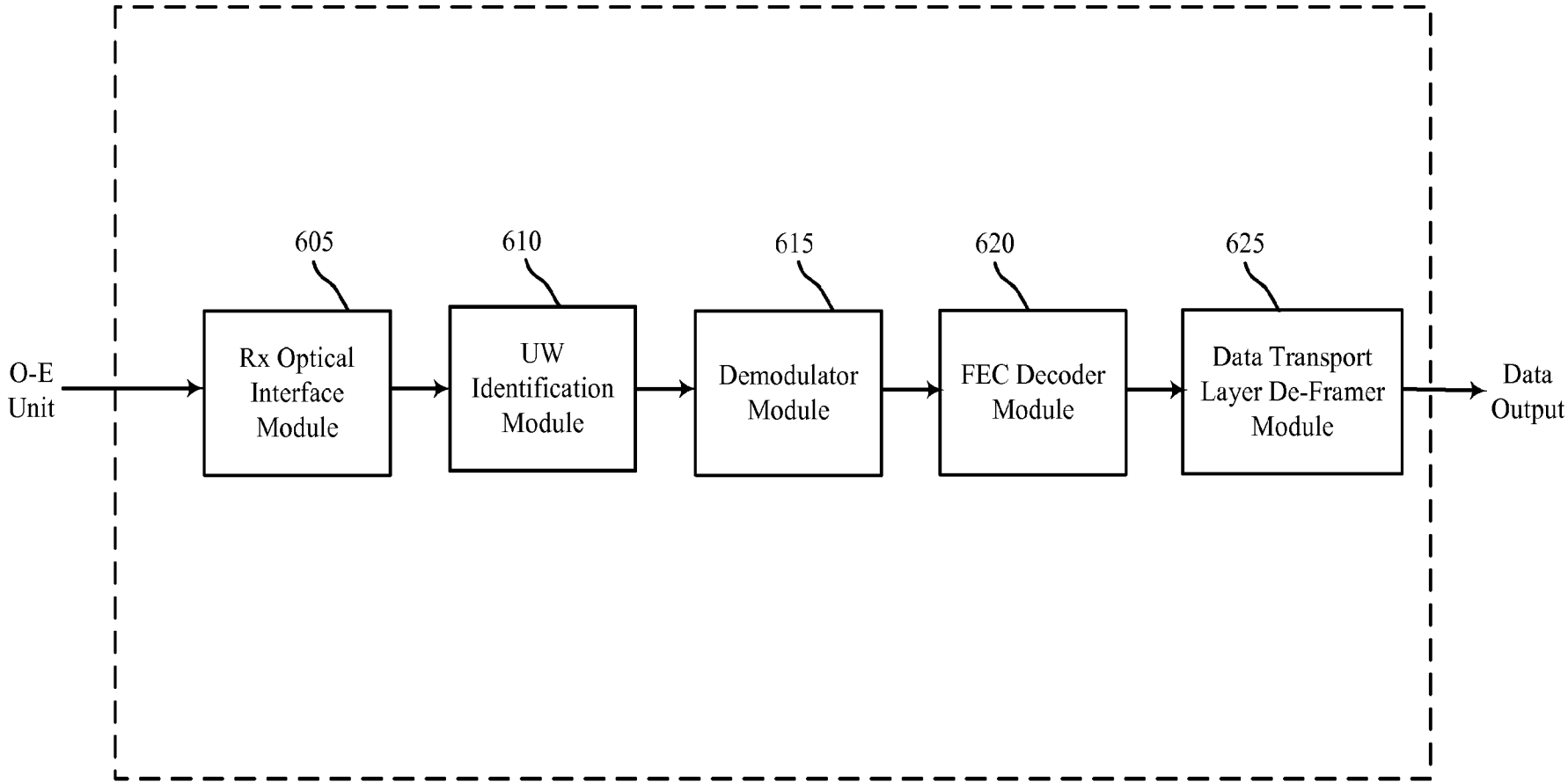

FIG. 6

Title: FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Inventor: Dave et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 6 of 9

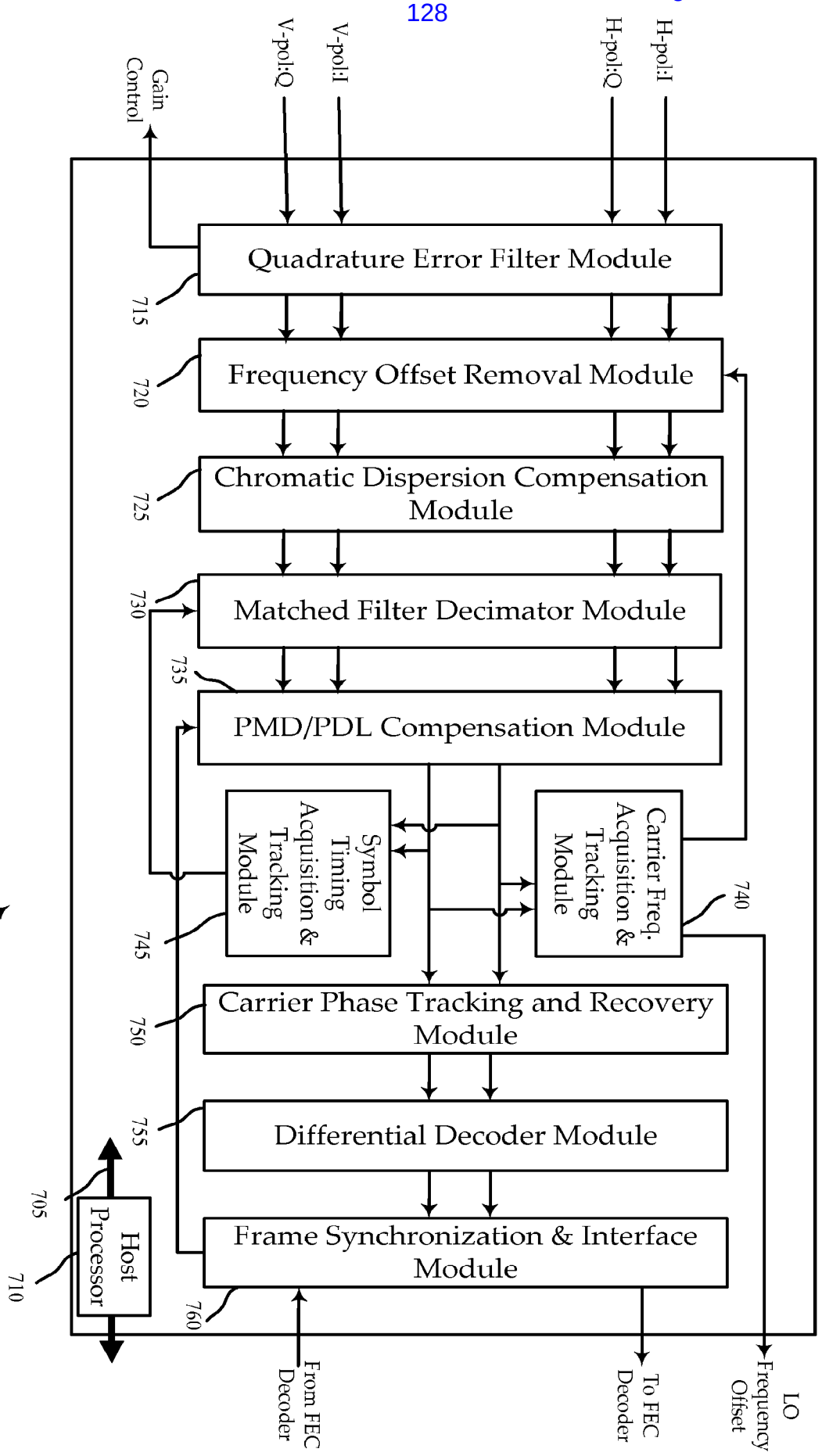

FIG. 7

700

Sheet 7 of 9

Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12

Title: FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Inventor: Dave et al.

[Exhibit 2-101]

Title: FRAME FORMATTING FOR HIGH-RATE OPTICAL COMMUNICATIONS
Inventors: Ive et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 8 of 9

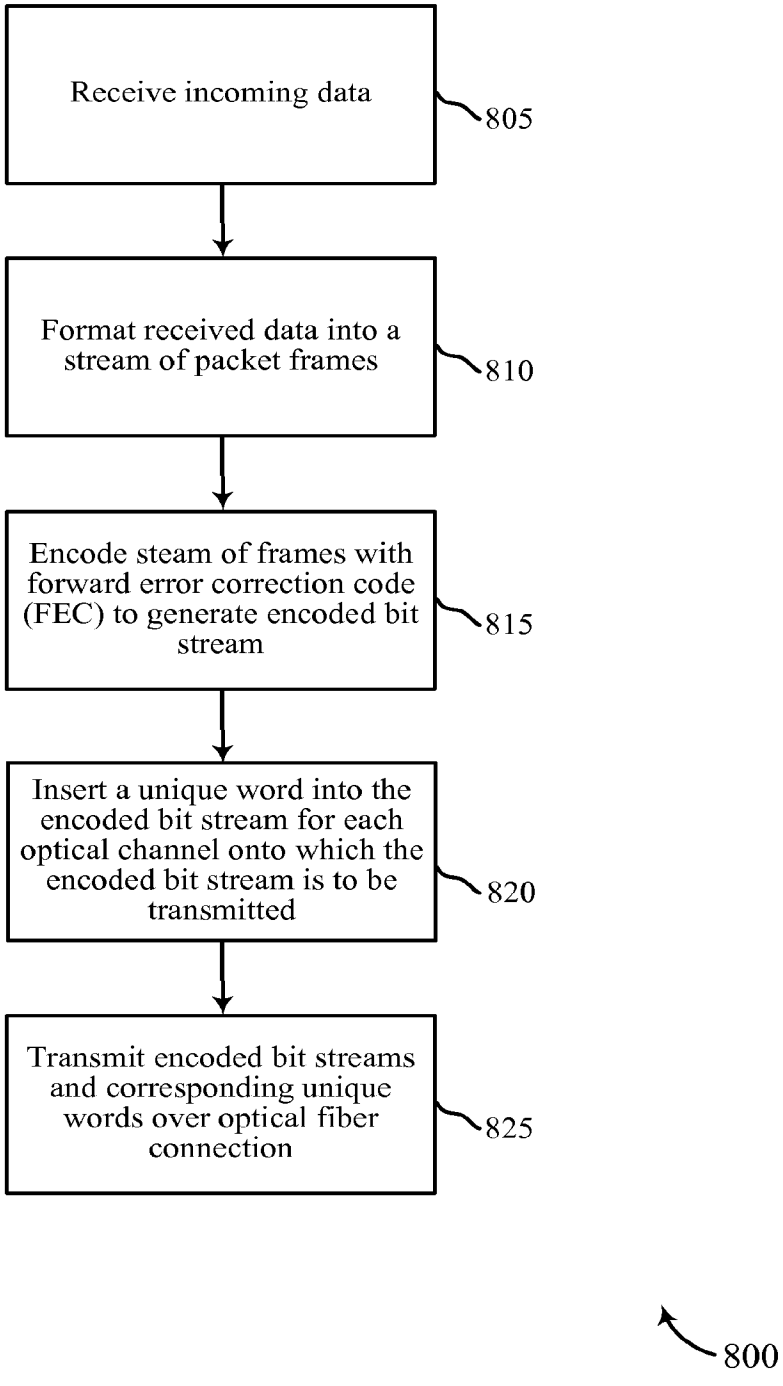

FIG. 8

Title: FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
Inventor: Olive et al.
Attorney Docket No.: P001.12 (78120.0014)
Client Ref. No.: FCC-0452-US-12
Sheet 9 of 9

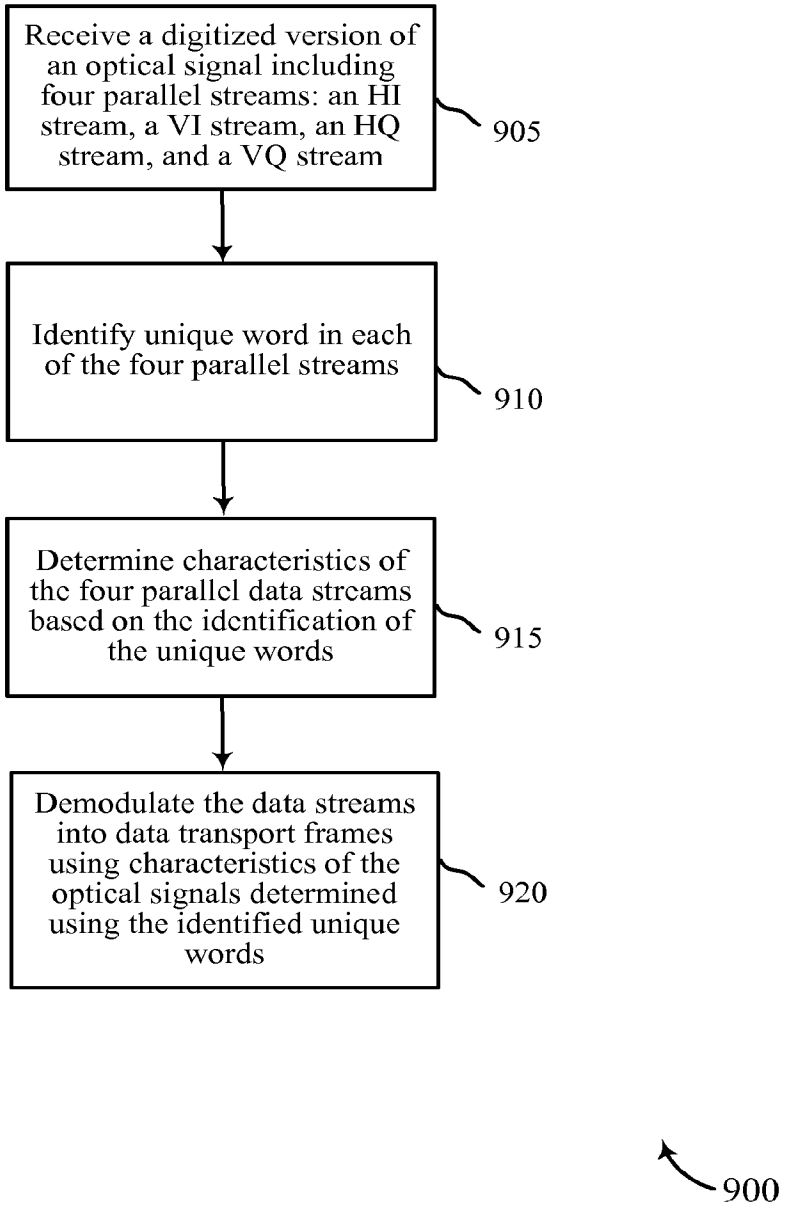

FIG. 9

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
First Named Inventor/Applicant Name:	Fan Mo
Filer:	Michael L. Drapkin/Sherry Soares
Attorney Docket Number:	P001.12 (78120.0014)

Filed as Large Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional application filing	1005	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

[Exhibit 2-104]

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**220**

Electronic Acknowledgement Receipt

EFS ID:	10690916
Application Number:	61521263
International Application Number:	
Confirmation Number:	1904
Title of Invention:	FRAME FORMATTING FOR HIGH RATE OPTICAL COMMUNICATIONS
First Named Inventor/Applicant Name:	Fan Mo
Customer Number:	16565
Filer:	Michael L. Drapkin/Sherry Soares
Filer Authorized By:	Michael L. Drapkin
Attorney Docket Number:	P001.12 (78120.0014)
Receipt Date:	08-AUG-2011
Filing Date:	
Time Stamp:	18:50:48
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$220
RAM confirmation Number	5578
Deposit Account	082623
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

[Exhibit 2-106]

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Provisional Cover Sheet (SB16)	P00112_78120-0014_ProvisionalCover.pdf	1060274 5fa3f5f1a6e5db8462b9131c182bcac6dc5758f2	no	3
Warnings:					
Information:					
2	Application Data Sheet	P00112_78120-0014_ADS.pdf	1031493 d85e93265f0f232b6cbe0a92f3344392ef64a608	no	4
Warnings:					
Information:					
3		P00112_78120-0014_Specification.pdf	116490 5374df3ebdf5782bc3179d46d624e3172be23fe0	yes	16

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	14
Claims	15	15
Abstract	16	16

Warnings:					
Information:					
4	Drawings-only black and white line drawings	P00112_78120-0014_Drawings.pdf	98960 aaf41f36093a2f0e817cec75a0b8bc3fd9af688a	no	9
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	29411 83b64827f1ebf469bda946333be533ec1bf607ae	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2336628		

[Exhibit 2-107]

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Exhibit 3

IP CORE DEVELOPMENT AND LICENSE AGREEMENT NO. TG11102009

This Agreement is entered into by and between ViaSat, Inc., a Delaware corporation having its headquarters offices located at 6155 El Camino Real, Carlsbad, California 92011-1699, and having a branch office located at 4830 East 49th Street, Cuyahoga Heights, Ohio 44125 (hereinafter referred to as "VIASAT") and Acacia Communications, Inc. a Delaware corporation having its principal place of business at 1000 Winter Street, Suite 4500, Waltham, Massachusetts 02451 (hereinafter referred to as "ACACIA"), as of the Effective Date defined in Clause 1.

WHEREAS VIASAT has extensive background and expertise in communications systems, and intellectual property core ("IP core") design and verification; including the successful incorporation of communications technology on a variety of platforms, such as Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs) programmable Digital Signal Processors (DSPs), and software (C/C++, Matlab, etc.).

WHEREAS ACACIA would like to commission VIASAT to undertake the development of an ASIC IP core for Digital Signal Processing (the "DSP Core") and an IP core for Soft Decision Forward Error Correction Decoder and Encoder (the "SDFEC Core") targeting an OTU4 (100Gb) optical transport application;

NOW, THEREFORE, in consideration of the mutual covenants and Agreements contained herein, VIASAT AND ACACIA agree as follows:

1. Definitions

As used in this Agreement the following defined terms shall have the meanings set forth below:

(a) "Affiliate" shall mean any company controlling, controlled by or under common control with a specified party, wherein "control" means the power to determine the management policies of such company by either ownership of a majority of the voting rights of its issued capital, or having the right to appoint a majority of the members of its board of directors, or by Agreement or otherwise.

(b) "Background Information" means all Intellectual Property Rights, and other design data and information either (a) owned or licensed by VIASAT prior to the Effective Date of this Agreement, or (b) developed or licensed by VIASAT separate and apart from this Agreement. Background Information shall also include all technical data, manuals and other documentation and data related to any of the foregoing. For the sake of clarity, and without limiting the foregoing, the SDFEC Core shall be deemed Background Information.

(c) "Copyrights" means copyrights and copyrightable works, in any form or medium now in existence or hereinafter created and all derivative works thereto, and all registrations, applications and renewals for any of the foregoing.

(d) "Deliverables" shall mean the deliverables provided by VIASAT to ACACIA pursuant to the Development Services. For the sake of clarity, the term Deliverable shall include all Foreground Information and Licensed Materials provided by VIASAT to ACACIA hereunder.

(e) "Development Services" shall have the meaning set forth in Clause 2(a).

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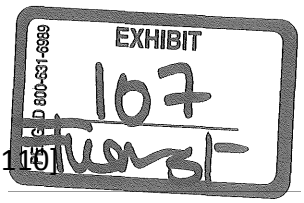

[Exhibit 3-116]

(f) "Effective Date" means the commencement date of this Agreement, and which shall be established as the last date signed by the Parties hereto on the last page of this Agreement.

(g) "End User" means an end user customer who purchases or agrees to purchase the Licensed Products.

(h) "Intellectual Property Rights" means any and all inventions (whether or not patentable and whether or not reduced to practice); patents and patent applications and continuations thereof; works of authorship and other copyrightable works; Copyrights; mask work rights; trade secrets (including, without limitation, data, ideas, formulae, compositions, manufacturing and production processes and techniques, know-how, research and development information, drawings, specifications, designs, plans, proposals, technical data, software (source and object code), financial, business and marketing plans, sales and promotional literature, customer and supplier lists and related information); information technologies (including, without limitation, software programs (both source and object code), data and related documentation); all other intellectual property rights throughout the world; and all copies and tangible embodiments of the foregoing in whatever form or medium.

(i) "Interim Agreement" means that certain Preliminary ASIC IP Core Development Agreement between the parties effective as of September 4, 2009.

(j) "Foreground Information" means all Intellectual Property Rights, design data and information (a) directly related to the Digital Signal Processing (DSP) Blocks for use in 100Gb Optical Systems described in Exhibit C hereof, entitled "Mutually Agreed Upon Specification for 100 Gbps Coherent DWDM Demodulator" to be delivered as part of Deliverable 2V/3A in Exhibit A, the Statement of Work (SOW), that are first developed or first created by VIASAT or its personnel during the course of performing services for ACACIA under this Agreement, or (b) that are first developed or first created by VIASAT or its personnel in the performance of its services relating to Digital Signal Processing under this Agreement, and including all changes, additions, revisions, replacements, manuals and documentation thereto which VIASAT may provide under this Agreement. For the sake of clarity, and without limiting the foregoing, the DSP Core and all Deliverables relating thereto shall be deemed Foreground Information.

(k) "Licensed Materials" means the SDFEC Core provided to ACACIA as part of the Development Services hereunder, in whatever form provided (whether as floppy or hard disks, cartridges, magnetic tapes, semiconductor chips or otherwise) or however designated (whether as firmware, microcode or otherwise) and including all changes, additions, revisions, replacements, manuals and documentation thereto which VIASAT may provide under this Agreement. For the avoidance of doubt, source code for Licensed Materials shall not be delivered to ACACIA under this Agreement and shall not be a Licensed Material.

(l) "Licensed Products" means any integrated circuits (ASIC and/or FPGA) designed, manufactured, marketed or sold by or on behalf of ACACIA that incorporate all or any part of the Licensed Materials (regardless of whether or not the Licensed Materials are enabled or disabled in such Licensed Product).

(m) "Royalty Bearing Products" means Licensed Products that incorporate all or part of the Licensed Materials regardless of whether or not the Licensed Materials are in an enabled form or disabled form.

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[Exhibit 3-111]

(n) "Permitted Use" means use by ACACIA of the Licensed Materials in accordance with Clause 4 below.

(o) "Recurring Royalty Fee" shall mean the per unit recurring royalty fee(s) payable to VIASAT by ACACIA under this Agreement as described in Clause 4 below.

(p) "Development Specifications" means the specifications made by ACACIA to VIASAT for the Foreground Information attached hereto and made a part of this Agreement as Exhibit C, which are mutually agreed to be considered draft specifications at the time of executing this Agreement, but which shall be converted to mutually agreeable final specifications in accordance with the process and timeline set forth in the SOW in Exhibit A.

(q) "Licensed Materials Specifications" means the specifications for the Licensed Materials set forth in Exhibit B.

(r) "Specifications" means the Development Specifications and the Licensed Materials Specifications, collectively.

2. IP Core Development Phase Scope, Price and Acceptance

(a) ViaSat will provide the necessary personnel, materials, services and facilities to perform the IP core development phase work (the "Development Services") specified in Exhibit A, entitled "Statement of Work for IP Core Development" which is attached hereto and made a part of this Agreement as Exhibit A. VIASAT shall perform the Development Services and deliver all Deliverables within the timeline set forth in Exhibit A.

(b) ViaSat will perform such Development Services for the NRE firm fixed price of Three Million Two Hundred Thousand Dollars ($3,200,000) (the "NRE Fee"), subject to such additional amounts for products or services set forth in Exhibit A regarding out-of-scope design iterations requested by ACACIA, which will be handled on a time and materials basis at rates set forth in Exhibit D or, if not set forth therein, as mutually agreed between the parties. Payments made by ACACIA to VIASAT pursuant to the Interim Agreement shall be credited toward the NRE Fee.

(c) VIASAT may invoice ACACIA for the NRE Fee upon completion of each payment milestone set forth in Exhibit A (hereafter referred to as a "Payment Milestone") and ACACIA's acceptance thereof in accordance with Clause 2(d). Payment associated with each successfully achievedPayment Milestone shall be payable within thirty (30) days after ACACIA's receipt of ViaSat's invoice. Any undisputed amounts not paid when due shall be subject to a late payment fee of one and one-half percent (1.5%) per month or the maximum amount permitted by law, whichever is less.

(d) Acceptance of the Development Services work shall occur after completion of acceptance tests in accordance with the SOW in Exhibit A. Acacia shall evaluate, and if applicable, conduct preliminary tests to verify conformance of each Deliverable to the applicable Specifications, and notify VIASAT of its acceptance within the applicable review time cycle(s) set forth in the SOW. If, within such applicable review time cycle ACACIA, in its good faith judgment, reasonably believes that any portion of the Deliverables does not conform to the applicable Specifications in any material respect, ACACIA shall within such applicable review time cycle deliver written notice to VIASAT of such non-conformity to the applicable

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Specifications ("Statement of Errors"), listing all discovered non-conformities. VIASAT shall use commercially reasonable efforts, at its own expense (except that if the non-conformity is due to any action or inaction on the part of ACACIA, in which case ACACIA shall bear the cost of correction) to correct such non-conformities within ten (10) business days but in no event longer than thirty (30) calendar days of its receipt of such a Statement of Errors. Upon receipt of the corrected Deliverable, ACACIA shall retest the Deliverable as set forth above. If ACACIA determines that the Deliverable still does not comply with the applicable Specifications in any material respect, ACACIA shall have the option of (a) rejecting the Deliverable as set forth above and asking VIASAT to repeat the corrective action described above, (b) agreeing upon a fix strategy with VIASAT (c) paying the associated Deliverable's Payment Milestone, if any, and proceeding to the next delivery milestone set forth in Exhibit A, or (d) terminating this Agreement upon written notice to VIASAT. In the event ACACIA has not (i) conducted any such acceptance tests or (ii) notified VIASAT as to any non-conformity within the applicable review time cycle(s) set forth in the SOW, such Deliverables shall be deemed accepted, unless the parties mutually agree in writing that circumstances warrant extending any such acceptance testing, which such agreement shall not be unreasonably withheld; in which case ViaSat and ACACIA will jointly develop a mutually agreeable extended acceptance test plan and a reasonable time period to be allowed for ACACIA to perform such extended acceptance test plan, taking into consideration the complexity of the extended acceptance testing to be performed.

(e) In the event that ACACIA terminates this Agreement pursuant to Clause 2(d)(d), VIASAT shall immediately cease performing additional Development Services and VIASAT shall be entitled to retain all amounts received to date, and a prorated amount for work performed toward the next to occur Payment Milestone. Notwithstanding anything to the contrary herein, in the event that ACACIA terminates this Agreement pursuant to Clause 2(d)(d) hereof all licenses hereunder, including without limitation licenses to the Licenses Materials, shall be terminated and revoked.

3. **Foreground Information**

(a) ACACIA shall own all right, title and interest in and to all Foreground Information, including all Intellectual Property Rights therein and thereto. VIASAT will promptly provide and fully disclose all Foreground Information to ACACIA. All Foreground Information is works made for hire to the extent allowed by law and, in addition, VIASAT, at ACACIA's sole expense, hereby makes and agrees to make all assignments necessary to accomplish the foregoing ownership. VIASAT shall assist ACACIA, at ACACIA's sole expense, to further evidence, record and perfect such assignments, and to perfect, obtain, maintain, enforce, and defend any rights assigned. If VIASAT is unavailable, unable or unwilling to so assist ACACIA, VIASAT hereby irrevocably designates and appoints ACACIA, solely in connection with the exercise of its ownership rights in the Foreground Information, as it agent and attorney in fact to act for and in VIASAT's behalf to execute and file any document and to do all other lawfully permitted acts to further the foregoing with the same legal force and effect as if executed by VIASAT.

(b) If any part of the Foreground Information is based on, incorporates or is an improvement or derivative of, or cannot be reasonably and fully made, used, reproduced, modified, distributed or otherwise exploited, without using any Background Information, then VIASAT hereby grants and agrees to grant to ACACIA a limited, nonexclusive, perpetual, irrevocable, worldwide, royalty-free, sublicensable right and license to make, have made, use and have used, sell, import, export, reproduce, modify and make derivative works of such Background Information for the sole and exclusive purpose of design, simulation, implementation, manufacture

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[Exhibit 3-113]

and sale of Licensed Products (including any modifications, improvements and derivatives to Licensed Products) or otherwise in connection with ACACIA's exploitation of the Foreground Information. VIASAT agrees not to use or disclose any Background Information under this Agreement for which it is not fully authorized to grant the foregoing license.

4. **License; Recurring License Fee; Licensed Material Delivery**

(a) VIASAT hereby grants to ACACIA for the Term of this Agreement a limited, worldwide, nonexclusive, non-transferable right and license (i) to make, have made, use, reproduce and make derivative works of the Licensed Materials, solely for the design, simulation, implementation and manufacture of Licensed Products, and (ii) to reproduce, make, have made, use, sell, offer to sell, import, export or otherwise distribute Licensed Products incorporating the Licensed Materials on a worldwide basis. Use of the Licensed Materials for any product other than the Licensed Product is strictly prohibited unless ACACIA has entered into a separate written Agreement with VIASAT for such use.

(b) The foregoing license is granted to ACACIA under this Agreement subject to: (i) ACACIA's full payment of all Development Services NRE amounts owed to VIASAT under Clause 2 above; and (ii) payment of a per unit Recurring Royalty Fee in accordance with the following table per each Royalty Bearing Product sold by or on behalf of ACACIA:

Recurring Royalty Fee		Cumulative Instantiation Quantity	Recurring Royalty Fee ($)	
		0 to 2,500	$750/instantiation	
		2,501-10,000	$500/instantiation	
		>10,000	$150/instantiation	

Notwithstanding anything to the contrary contained in this Agreement, no Recurring Royalty Fee shall be due for Licensed Products that are: (i) used or distributed solely for internal use by ACACIA (except any subsequent sale of the same would bear such Recurring Royalty Fee), (ii) used or distributed solely for demonstration, marketing or training purposes (except any subsequent sale of the same would bear such Recurring Royalty Fee), provided such use and distribution shall be limited to an aggregate of fifty (50) units, (iii) distributed to an End User as a replacement for a defective Licensed Product or to fix an error in a Licensed Product (but only to the extent a Recurring Royalty Fee was paid on the original Licensed Product so replaced or corrected), (iv) returned by an End User (except only to the extent a complete refund of the purchase price is made by ACACIA to such End User), or (v) used solely for ACACIA's manufacturing or testing purposes.

(c) Restricted Activities. As additional protection for Acacia's Confidential Information, VIASAT agrees that during the period over which it is (or is supposed to be) providing Development Services under this Agreement (i) and for six (6) months thereafter (the "Restricted Period"), ViaSat will not (i) engage in activities related to the Foreground Information which are directly competitive with the 100Gb transponder module business or demonstrably anticipated 100Gb transponder business of ACACIA or (ii) provide services related to the "Foreground Information" to (a) any third parties in the 100Gb optical transponder module market who are engaged in activities directly competitive with the 100Gb transponder business or demonstrably anticipated 100Gb transponder business of ACACIA or (b) any third party that is or

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[Exhibit 3-114]

was previously a customer or business partner of ACACIA if such services are in support of the 100Gb optical transponder module market.

5. Taxes

All international, national, regional or local taxes, duties or similar liabilities, however designated, except for income taxes imposed by the U.S. Government or its political subdivisions, which may be levied upon VIASAT in connection with this Agreement (excluding taxes based on VIASAT's income) shall be for the account of ACACIA and paid directly by ACACIA or, if required to be paid by VIASAT, shall be immediately reimbursed by ACACIA to VIASAT upon evidence of payment.

6. **Accounting and Payment for Recurring Royalties**

(a) During the Term ACACIA shall keep accurate, separate and complete records in sufficient detail to enable the payments due hereunder to be determined (and to permit and allow ViaSat to confirm the same pursuant to Clause 6(c)).

(b) Within thirty (30) days after the end of each calendar quarter during the Term of this Agreement, beginning with the first calendar quarter after ACACIA completes development of its first prototype of a Licensed Product, ACACIA shall transmit a written report to VIASAT with respect to accounting for all Recurring Royalty Fee payments due hereunder. Such report shall indicate (i) the quantity of Royalty Bearing Products shipped during the reporting quarter, (ii) the per unit Recurring Royalty Fee attributable to such Royalty Bearing Products as set forth in Clause 4 above, (iii) the cumulative Recurring Royalty Fees owed to VIASAT for such period and (iv) such other reasonable information requested by VIASAT from time to time. If no such sales have been made during any reporting period, ACACIA shall so report. Contemporaneously with submitting each such quarterly report, ACACIA shall submit its payment for all reported Recurring Royalty Fees in cash by means of electronic wire transfer using the following instructions:

Electronic Wire Transfer Instructions

Bank:	Union Bank of California
Address:	530 "B" Street San Diego, CA 92101-4407 USA
Routing Transit #:	122000496
Acct Name:	ViaSat, Inc. General Checking Account
Acct #:	4000142625
Swift ID:	BOFC US 33 MPK (For international wire transfers)

Any Recurring Royalty Fees which are not paid by ACACIA within thirty (30) days after the close of the calendar quarter in which ACACIA received the revenue attributable to such Royalty Bearing Product shall be subject to a late payment fee of one and one-half percent (1.5%) per month or the maximum percent permitted by law, whichever is less.

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[Exhibit 3-115]

(c) Upon seven days written notice from the VIASAT, ACACIA shall permit an independent certified public accountant, reasonably acceptable to ACACIA, to have access, no more than once each calendar year during regular business hours, to such records or documents of ACACIA as may be necessary to verify the accuracy of the reports and payments made under this Agreement, including but not limited to, invoices, contracts and purchase orders, and to make copies thereof. The cost of such audit shall be at VIASAT's sole cost and expense, except if the review uncovers an underreporting in the reported license fees or other amounts due of more than five percent (5%), in which case ACACIA shall promptly pay to VIASAT (i) such underreported or unpaid amount plus (ii) the cost of said audit.

7. Term; Termination

(a) The term of this Agreement shall commence as of the Effective Date and shall continue until terminated as set forth in this Clause 7 ("Term").

(b) ACACIA may terminate this Agreement for any reason at any time upon thirty (30) days prior written notice to VIASAT. In the event that ACACIA terminates this Agreement pursuant to this Clause 7(b), VIASAT shall immediately cease performing additional Development Services and VIASAT shall be entitled to retain all amounts received to date, plus ACACIA shall promptly pay to VIASAT (i) a prorated amount for work performed toward the next to occur Payment Milestone plus (ii) any non-cancellable expenses incurred by VIASAT prior to receipt of ACACIA's notice of termination plus (iii) any other amounts due and payable.

(c) Either party may terminate this Agreement based on material breach of the Agreement by the other party, provided that, for any breach capable of cure, the party alleged to be in material breach receives written notice stating the cause and is provided thirty (30) days to cure such material breach. In the event of termination pursuant to this Clause 7(c), any payment obligations accruing prior to such termination will remain due and owing and VIASAT shall be entitled to seek injunctive relief allowing VIASAT to recover from ACACIA any Licensed Materials already delivered to ACACIA, in addition to any other remedies available, it being acknowledged that legal remedies may be inadequate.

(d) Upon termination of this Agreement, (i) except as expressly set forth below, the licenses, rights and covenants granted hereunder and the obligations imposed hereunder will cease; (ii) ACACIA will destroy the Licensed Materials, including all copies and all relevant documentation and within ten days of termination provide written certification of such destruction to VIASAT, except that, if this Agreement is terminated for any reason other than ACACIA's material breach thereof, ACACIA may sell any Licensed Products already in inventory as of the effective date of Termination subject to payment of the applicable Recurring Royalty Fee for any Royalty Bearing Products sold. The provisions of Clauses 1, 3, 8, 9, 11, 12, 13, 14, 18, 19 and this Clause 7(d) will survive the termination of this Agreement.

8. Background Information Title; Intellectual Property Rights; Copying

(a) ACACIA acknowledges that all Intellectual Property Rights in the Background Information and the Licensed Materials are and will remain the sole property of VIASAT, including all modifications, improvements, and derivative works relating to the Background Information and the Licensed Materials, including but not limited to all modifications, improvements, and derivative works requested or suggested by ACACIA.

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[Exhibit 3-116]

(b) To protect such Intellectual Property Rights, ACACIA agrees that it will use any Background Information and/or Licensed Materials it receives from VIASAT under this Agreement only as authorized herein and for the term specified herein and agrees that it will not decompile, reverse engineer, disassemble, or otherwise reduce any Background Information and/or Licensed Materials it receives from VIASAT under this Agreement to a human-perceivable form except to the extent any of the foregoing restrictions are prohibited by law. ACACIA may not modify or prepare derivative works of any Background Information and/or Licensed Materials it receives from VIASAT under this Agreement in whole or in part, except with respect to the purposes of the Licensed Products. Nothing contained in this Agreement will be construed as conferring by implication, estoppel or otherwise upon either party any license or other right except the licenses and rights expressly granted in this Agreement to a party hereto. ACACIA acknowledges that any Background Information and/or Licensed Materials it receives from VIASAT under this Agreement represents valuable property of VIASAT, and may be protected by copyright law.

(c) This Agreement allows ACACIA to copy any Background Information and/or Licensed Materials it receives from VIASAT under this Agreement only to the extent expressly provided herein, and for archival and back-up purposes, provided always that ACACIA will at all times and in each instance, reproduce all copyright notices and proprietary legends on each copy in the same manner as such notices and legends appeared on the original. No other copies may be made without VIASAT's prior written consent. ACACIA may not provide design data or information including, but not limited to, schematics, hardware description language source code, or netlist files, to a third party without prior written approval from VIASAT.

9. **Confidentiality**

Each Party shall maintain in strict confidence, and will use and disclose only as authorized by the disclosing party, in accordance with the provisions of Non-Disclosure Agreement #NDATG06102009 executed between them on June 10, 2009 (the "NDA"), all information that it receives from the other Party in connection with this Agreement (including pursuant to a SOW), including, but not limited to, all information concerning trade secrets, engineering, material, supplies, hardware, equipment, software or other technical information of the other Party's products or financial, accounting or marketing information, business plans, analyses, forecasts, predictions or projections, and customer information relating to the other Party's business, and personnel information relating to the other Party's employees (hereinafter referred to as "Confidential Information"). All Foreground Information shall be deemed ACACIA's Confidential Information for purposes of the NDA. The terms of this Clause 9 shall survive the termination of this Agreement.

10. **Right to Transfer to the U.S. Government**

For any Licensed Materials subsequently ordered from ACACIA under a U.S. Government prime contract or subcontract (of any tier), ACACIA shall have the right, upon written prior notice to VIASAT, and subject to the limits of the license rights granted under this Agreement, to transfer said Licensed Materials to the U.S. Government provided that the Government agrees to accept said transfers subject to Restricted Rights as such rights are defined and limited by the Rights in Technical Data and Computer Software clause in DFARS 252.227-7013.

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[Exhibit 3-117]

11. Indemnity

VIASAT will defend, protect, indemnify and hold ACACIA and its officers, directors, and employees and its affiliates and their respective officers, directors, and employees, harmless from and against any and all third party demands, claims, liabilities, losses, costs and expenses (including reasonable attorneys' fees), losses or damages to persons or property, injuries or death of persons (including the amounts of judgments, settlement amounts, penalties, interest, court costs and legal fees, including on appeal or review) arising out of or relating to any negligent act or omission, or default by VIASAT or its personnel under this Agreement.

12. Warranties, Limited Remedy and Disclaimer.

(a) VIASAT represents warrants to ACACIA that: (i) VIASAT has and shall have all rights necessary to grant the rights and licenses granted hereunder; (ii) VIASAT has the required skills, expertise and experience to perform this Agreement; and (iii) VIASAT's performance of its obligations under this Agreement shall at all times comply with any and all applicable material laws and regulations.

(b) VIASAT represents and warrants that, for a period of one (1) year after ACACIA's commencement of production of Licensed Products (the "Warranty Period"), the Licensed Materials and Foreground Information will conform to the Specifications in all material respects and be free from material defects in design, manufacture, engineering, materials and workmanship. In the event the Licensed Materials and Foreground Information fail to meet the Specifications in all material respects, VIASAT shall repair or replace the non-conforming Licensed Materials or Foreground Information. VIASAT's sole liability and the ACACIA's exclusive remedy with respect of breach of the foregoing limited representation will be limited to error correction or replacement.

(c) EXCEPT AS SPECIFICALLY STATED IN THIS CLAUSE 12, THE LICENSED MATERIALS LICENSED HEREUNDER ARE PROVIDED WITHOUT ANY OTHER WARRANTY OF ANY KIND, EITHER EXPRESSED, IMPLIED OR STATUTORY, INCLUDING WITHOUT LIMITATION, ANY WARRANTY WITH RESPECT TO NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

13. Limitations of Liability

EXCEPT FOR BREACHES OF CLAUSE 9 (CONFIDENTIALITY) OR THE NDA, OR AMOUNTS PAYABLE TO THIRD PARTIES PURSUANT TO CLAUSE 11 (INDEMNITY), (A) IN NO EVENT SHALL EITHER PARTY BE LIABLE TO THE OTHER PARTY FOR LOSS OF PROFITS OR INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES RESULTING FROM OR ARISING OUT OF OR IN CONNECTION WITH THIS AGREEMENT, WHETHER OR NOT SUCH PARTY HAD BEEN ADVISED, KNEW OR SHOULD HAVE KNOWN OF THE POSSIBILITY OF SUCH DAMAGES, INCLUDING, BUT NOT LIMITED TO, LOSS OF DATA, LOSS OF USE OR LOSS OF REVENUE, AND (B) EXCEPT FOR VIASAT'S OBLIGATION TO CORRECT DEFECTIVE LICENSED MATERIALS AND FOREGROUND INFORMATION PURSUANT TO CLAUSE 12, THE TOTAL CUMULATIVE LIABILITY OF EITHER PARTY UNDER THIS AGREEMENT, WHETHER ARISING

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[Exhibit 3-118]

OUT OF BREACH OF CONTRACT (INCLUDING BUT NOT LIMITED TO BREACH OF WARRANTY) OR TORT (INCLUDING BUT NOT LIMITED TO NEGLIGENCE AND STRICT LIABILITY), IN NO EVENT SHALL EXCEED THE AGGREGATE AMOUNT PAID BY ACACIA TO VIASAT PURSUANT TO THIS AGREEMENT.

14. Import/Export

ACACIA agrees to comply with all applicable U.S. import/export laws and regulations regarding the Licensed Materials including, but not limited to, the Arms Export Control Act (22 USC 2751 et seq.), the International Traffic in Arms Regulations (22 CFR Part 120 et seq.), and the Export Administration Act (50 USC 2401 et seq.). Without limiting the foregoing, ACACIA agrees that it will not transfer any export controlled-item, data or services to any third party without an export license, Agreement, or applicable exemption or exception.

15. Notices

All formal contractual notices under this Agreement shall be sent via email or facsimile and confirmed with a signed copy sent by regular mail as follows:

ViaSat, Inc.
Russell Fuerst, Vice President
4830 East 49th Street
Cuyahoga Heights, Ohio 44125
Phone: (216) 706-7619
Fax: (216) 441-8860
Russell.fuerst@viasat.com

Acacia Communications, Inc.
Bhupen Shah
1000 Winter Street, Suite 4500
Waltham, Massachusetts 02451
Phone: (617) 510-1411
Fax:
bhupen.shah@acacia-inc.com

With a copy sent to:

ViaSat, Inc.
Ted Gammell, Director, Contracts
20511 Seneca Meadows Parkway, Suite 200
Germantown, Maryland 20876

(240) 686-4490
(240) 686-4810
ted.gammell@viasat.com

Acacia Communications, Inc.
Marc F. Dupré, Esq.
Gunderson Dettmer LLP
610 Lincoln Street
Waltham, MA 02451
781-890-8800
781-622-1622
mdupre@gunder.com

Either party may change the above points of contact or addresses by seven (7) days prior written notice to the other party.

16. Entire Agreement

This Agreement and the NDA, and any referenced attachments thereto, contains the entire understanding between the parties, superseding any and all prior and contemporaneous communications, agreements and understandings between the parties with respect to the subject matter hereof. For the sake of clarity, and without limiting the foregoing, this Agreement shall supersede and replace the Interim Agreement. This Agreement may be executed in one or more counterparts, each of which is an original, but together constituting one and the same instrument.

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[Exhibit 3-119]

Execution of a facsimile copy shall have the same force and effect as execution of an original, and a facsimile signature shall be deemed an original and valid signature.

17. Assignment and Parties of Interest

Except as may be expressly authorized elsewhere herein, neither this Agreement nor any rights granted hereunder may be sold, assigned or transferred by a Party in any manner without the prior written consent of the other Party, which consent will not be unreasonably withheld, conditioned or delayed. Notwithstanding the foregoing, each Party will, without consent of the other Party, have the right to assign all or any part of its rights and obligations under this Agreement to any successor to all or substantially all of its business that concerns this Agreement (whether in connection with a merger, consolidation, or sale of all or substantially all of the assets or stock of the assigning Party). This Agreement will inure to the benefit of, and be binding upon, VIASAT and ACACIA, their successors and permitted assigns. This Agreement is enforceable only by VIASAT and ACACIA. The terms of this Agreement are not a contract or assurance regarding compensation, continued employment, or benefit of any kind to any of VIASAT's personnel assigned to ACACIA's work, or any beneficiary of any such personnel, and no such personnel, or any beneficiary thereof, will be a third-party beneficiary under or pursuant to the terms of this Agreement. The parties shall be independent contractors in their performance under this Agreement, and nothing contained herein will constitute either party as the employer, employee, agent or representative of the other party, or both parties as joint venturers or partners for any purpose.

18. Severability

If any provision of this Agreement or any portion or provision hereof applicable to any particular situation or circumstance is held invalid, the remainder of this Agreement or the remainder of such provision (as the case may be), and the application thereof to other situations or circumstances, will not be affected thereby.

19. Choice of Law

This Agreement shall be governed by the laws of the State of Delaware, without regard to its principles of conflict of laws. The United Nations International Sale of Goods Convention shall not apply to this Agreement.

20. Force Majeure

Neither party shall not be liable for any loss, damage, detention, or delay resulting from failure to perform under this Agreement due to causes beyond such party's reasonable control, including, but not limited to, acts of God or of the public enemy, acts of the Government in either its sovereign or contractual capacity, fires, floods, epidemics, quarantine restrictions, strikes, labor disputes, embargoes, unusually severe weather, insurrection or riot. In the event of delay resulting from any such causes, an equitable adjustment shall be made in the prices set forth in this Agreement (if warranted by the delay) and the performance dates hereof shall be extended for a reasonable length of time (if warranted by the delay) , but no event for less than the period of delay.

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[Exhibit 3-120]

21. Indemnity for Intellectual Property Infringement

(a) VIASAT agrees defend and hold harmless ACACIA from and against any claims, liabilities or actions and to pay all costs, losses, damages, settlement amounts and attorneys' fees incurred in connection with any claim by a third party against ACACIA to the extent that such claim alleges that the design or the construction of a Deliverable, as furnished by VIASAT under this Agreement, infringes the U.S. Intellectual Property Rights of such third party, provided that ACACIA promptly notifies VIASAT, in writing, of such claims (except that any delay or failure in notification shall not relieve VIASAT of its obligations except to the extent it has been prejudiced thereby), and provided ACACIA gives VIASAT the sole right to defend and settle such claim at VIASAT's expense with counsel of VIASAT's choice (provided that ACACIA may participate in the defense and settlement of any such claim with counsel of its own choosing at its own expense). ACACIA shall cooperate with VIASAT in the defense or settlement of the claim.

(b) If the manufacture, use or sale of a Deliverable is enjoined, VIASAT shall, at VIASAT's expense, to do one of the following: (a) obtain for ACACIA the right to use the allegedly infringing Deliverable, (b) modify the allegedly infringing Deliverable so that it becomes non-infringing or (c) replace the allegedly infringing Deliverable with a non-infringing Deliverable that is substantially in compliance with the Specifications for the alleged infringing Deliverable in all material respects. If VIASAT believes a Deliverable is likely to be the subject of a claim, suit, proceeding or injunction, VIASAT shall also have the right, at VIASAT's option, to do any of the above. If VIASAT elects to replace an allegedly infringing Deliverable with a non-infringing item, ACACIA shall return the allegedly infringing Deliverable to VIASAT as soon as practicable.

(c) Under no circumstances shall VIASAT have any liability for infringement to the extent such infringement arises from or occurs as a result of (i) the use of the Deliverables in combination and/or configuration with other items not furnished by VIASAT, (ii) incorporation of a specific design or modification at the request of ACACIA, (iii) Intellectual Property Rights owned by ACACIA or (iv) the failure by ACACIA to implement changes, replacements or new releases recommended by VIASAT, where the infringement would have been avoided by such changes, replacements or new releases and such changes would not have substantially impaired the functionality of the Deliverable. ACACIA agrees defend and hold harmless VIASAT from and against any claims, liabilities or actions and to pay all costs, losses, damages, settlement amounts and attorneys' fees incurred in connection with any claim by a third party against VIASAT to the extent that such claim arises out of any of the foregoing, provided that VIASAT promptly notifies ACACIA, in writing, of such claims (except that any delay or failure in notification shall not relieve ACACIA of its obligations except to the extent it has been prejudiced thereby), and provided VIASAT gives ACACIA the sole right to defend and settle such claim at ACACIA's expense with counsel of ACACIA's choice (provided that VIASAT may participate in the defense and settlement of any such claim with counsel of its own choosing at its own expense). VIASAT shall cooperate with ACACIA in the defense or settlement of the claim.

(d) This Clause 21 specifies each party's entire liability with respect to infringement of third party Intellectual Property Rights. VIASAT makes no warranty of non-infringement, express or implied. Notwithstanding Clause 13, ViaSat's total liability for the cost of any award of damages and costs, or settlement arising under this Clause 21 shall not exceed an amount equal to two (2) times the aggregate amount paid by Acacia to ViaSat pursuant to this Agreement. The existence of one or more claims or lawsuits shall not exceed this amount.

TMG
11/13/09

CR
11/20/09

[Exhibit 3-121]

22. **Modification and Waiver**

This Agreement may only be modified or amended in a writing signed by an authorized representative of each party. A waiver or failure to exercise any right provided for in this Agreement in any respect shall not be deemed a waiver of any further or future rights hereunder. Except as specifically provided otherwise, each right and remedy in this Agreement is in addition to any other right or remedy, at law or in equity, and the exercise of one right or remedy will not be deemed a waiver of any other right or remedy.

IN WITNESS WHEREOF, the parties have caused this Agreement to be duly executed in duplicate originals by their duly authorized representatives on the day and year first above written.

VIASAT, INC.	ACACIA COMMUNICATIONS, INC.
Signature (*):	Signature (*):
Name: Ted M. Gammell	Name: Christian Rasmussen
Title: Director, Contracts	Title: President
Date: November 13, 2009	Date: November 20, 2009

(*) - Delivery of an executed counterpart of a signature page to this Agreement by facsimile or email shall be effective as delivery of a manually executed counterpart of this Agreement.

TMG 11/13/09

CR 11/20/09

[Exhibit 3-122]

EXHIBIT 4

(THIS EXHIBIT IS SUBJECT TO A MOTION TO FILE UNDER SEAL)

EXHIBIT 5

(THIS EXHIBIT IS SUBJECT TO A MOTION TO FILE UNDER SEAL)